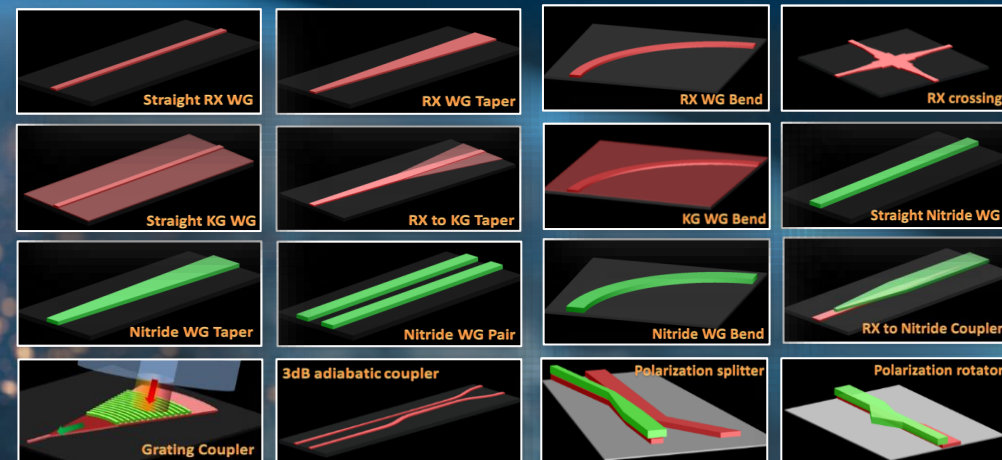
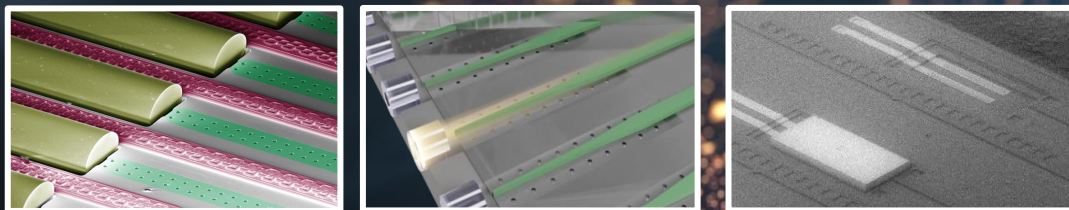
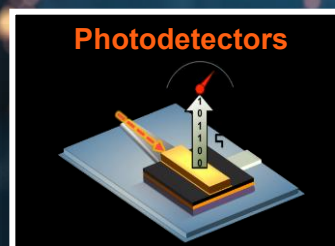
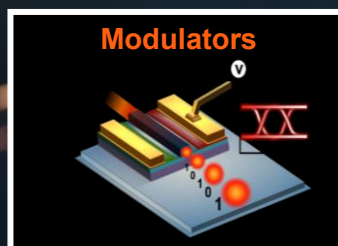
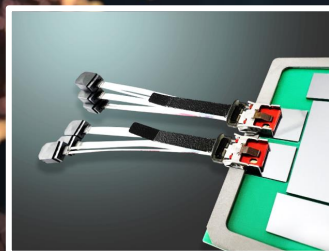
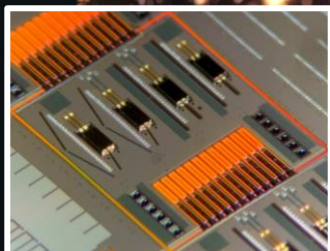




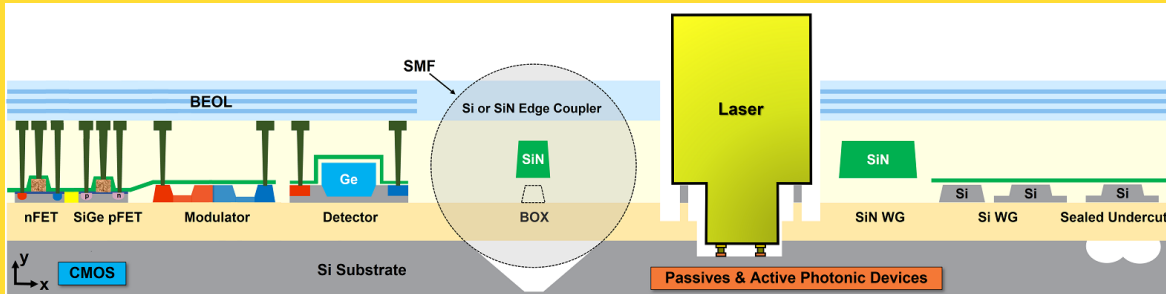
300-mm Monolithic Silicon Photonics Foundry Technology



Yusheng Bian*, PhD
GlobalFoundries
Director/DMTS
*yusheng.bian@gf.com

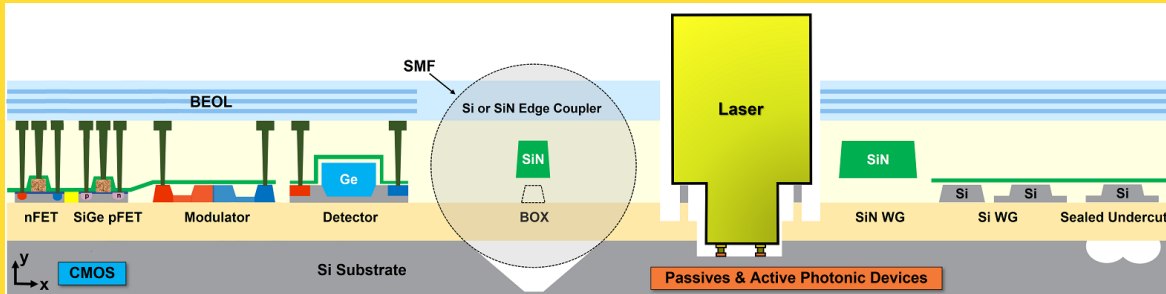
Oct, 2025

Outline



- ❑ GF & 45SPCLO Technology Overview
- ❑ Photonics Device Library and Enhancements
- ❑ Edge couplers and Advanced Packaging
- ❑ Fotonix™ PDK Enhancements
- ❑ System-level Analyses and Circuit Demonstrations
- ❑ Summary and Outlook

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GF Fotonix™: Trusted Production Solution

GlobalFoundries (GF) is the world's third-largest semiconductor foundry by revenue

Fab8 Malta, NY



Market
Segments

Computing, mobile,
wired and wireless
infrastructure.
Trusted Foundry



Employees

~3,000



Differentiated
Technologies

14/12LP, 12LP+,
12RF, 45RF
Silicon Photonics



Operating since

2011

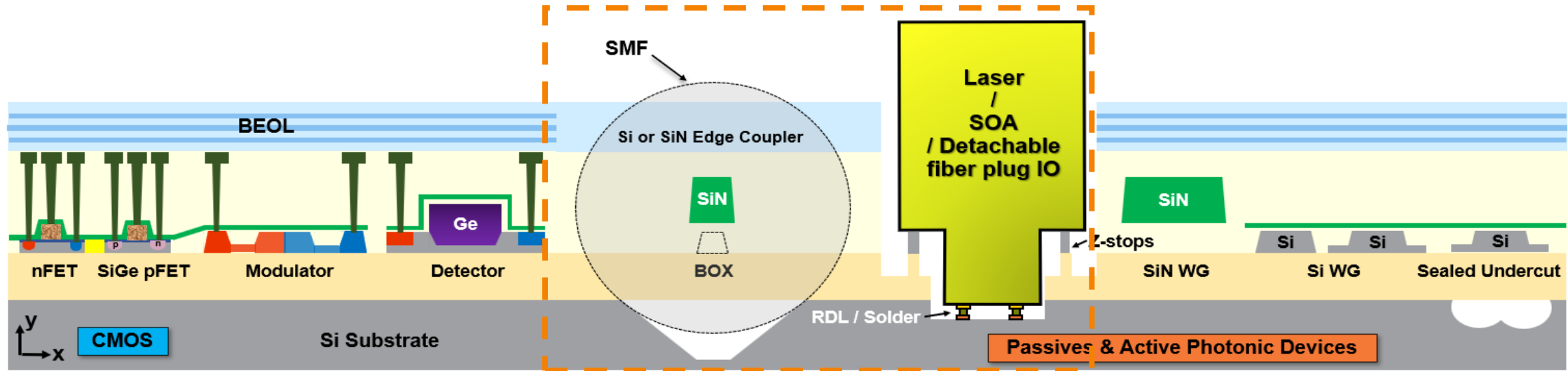


Manufacturing
capacity

500k
(300mm wafers/year)

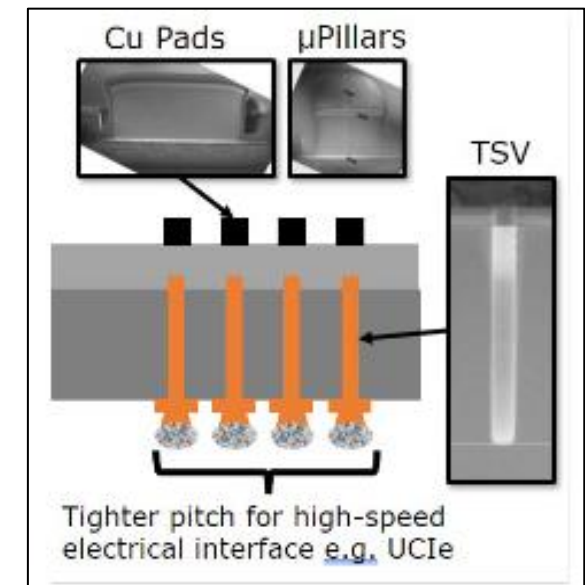


GF monolithic SiPh platform overview



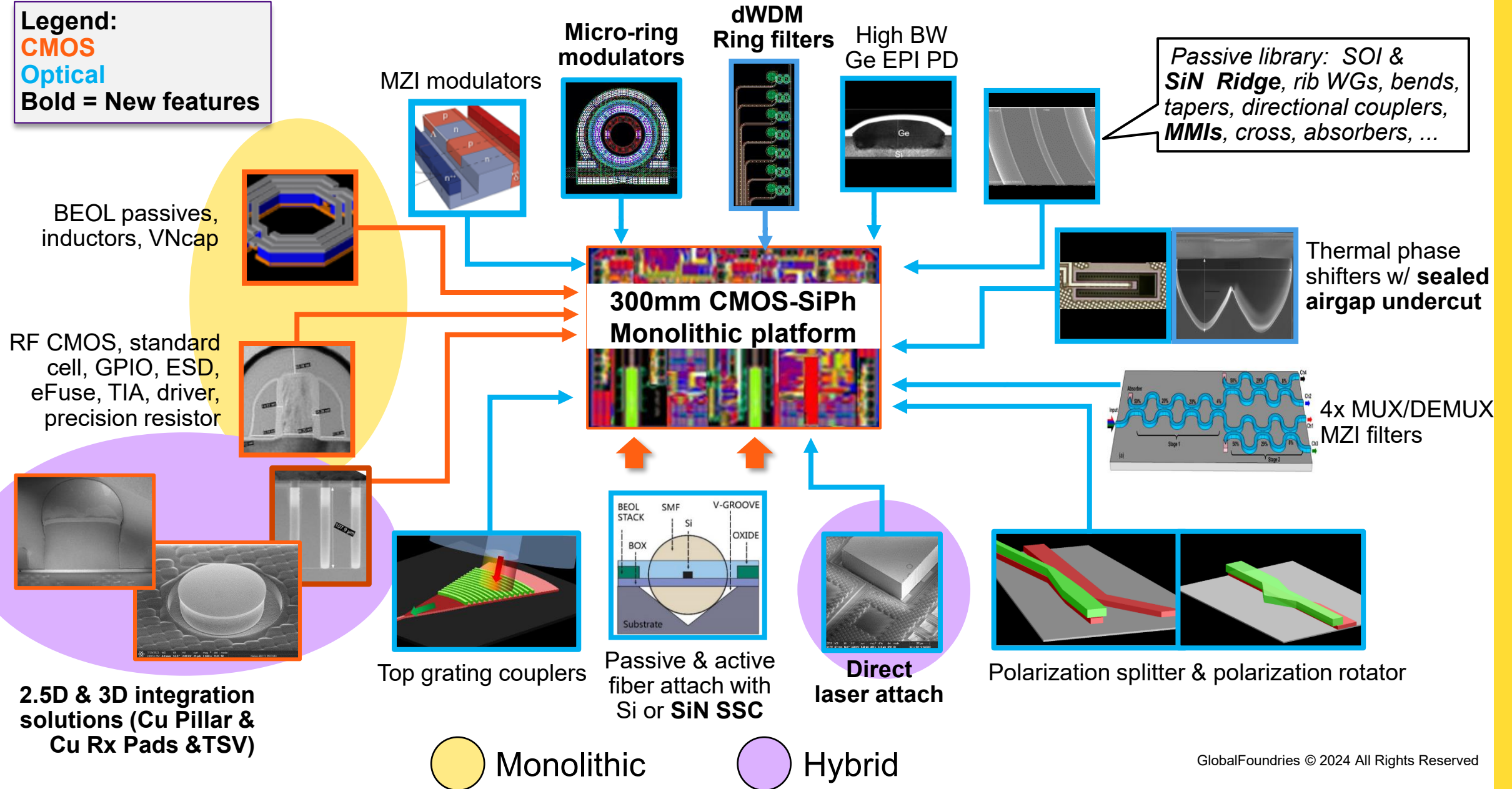
Source: Y. Bian, et al., IEEE JSTQE, 29(3) 8200519 (2023)

- **Monolithic integration of 45nm class RFCMOS & std cell digital logic**
- **Fiber Attach:** 250/127um pitch passive V-groove, 32+ array size
- **Photonic Device Highlights**
 - Comprehensive O-band photonic library
 - 56Gbaud PD and modulators. 112Gbaud in development (**120 Gbaud PD – CLEO 2025 PDP**)
 - 300GHz class analog mixed signal CMOS with standard cell digital library
 - Enhanced high power SiN device suite, including athermal cWDM
 - Micro-ring dWDM ring filters with high efficiency sealed undercut (airgap) heaters
 - Polarization management, PSRs, low PDL
- **Cu Pillar & TSV** (<55um pitch) supports 2.5D & 3D form-factors
- **Flows support hybrid EIC** only or as combination of hybrid EIC + monolithic EPIC
- **State-of-art Co-design PDK:** Hardware-based models, 105C, self-heating, optical power
- **Custom design support:** freeform / curve-linear GDS accepted, stack-up guide
- **300mm patterning:** immersion lithography Si WG, Optimized OPC for photonic layouts

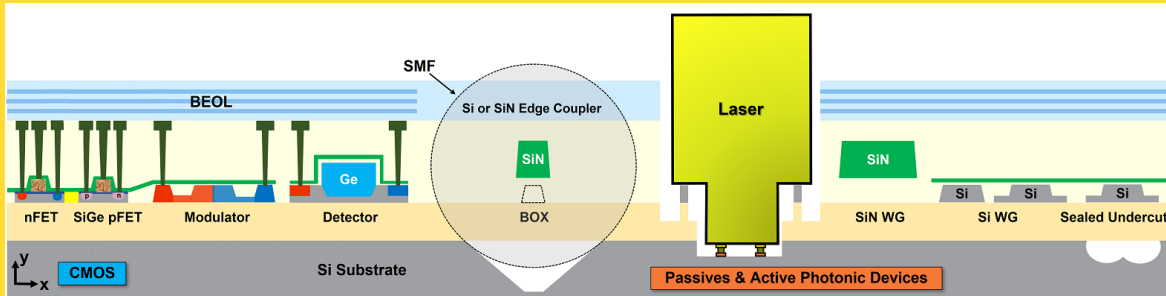


GF Fotonix™: Technology Solution

Legend:
CMOS
Optical
Bold = New features



Outline



- ❑ GF & 45SPCLO Technology Overview

- ❑ **Photonics Device Library and Enhancements**

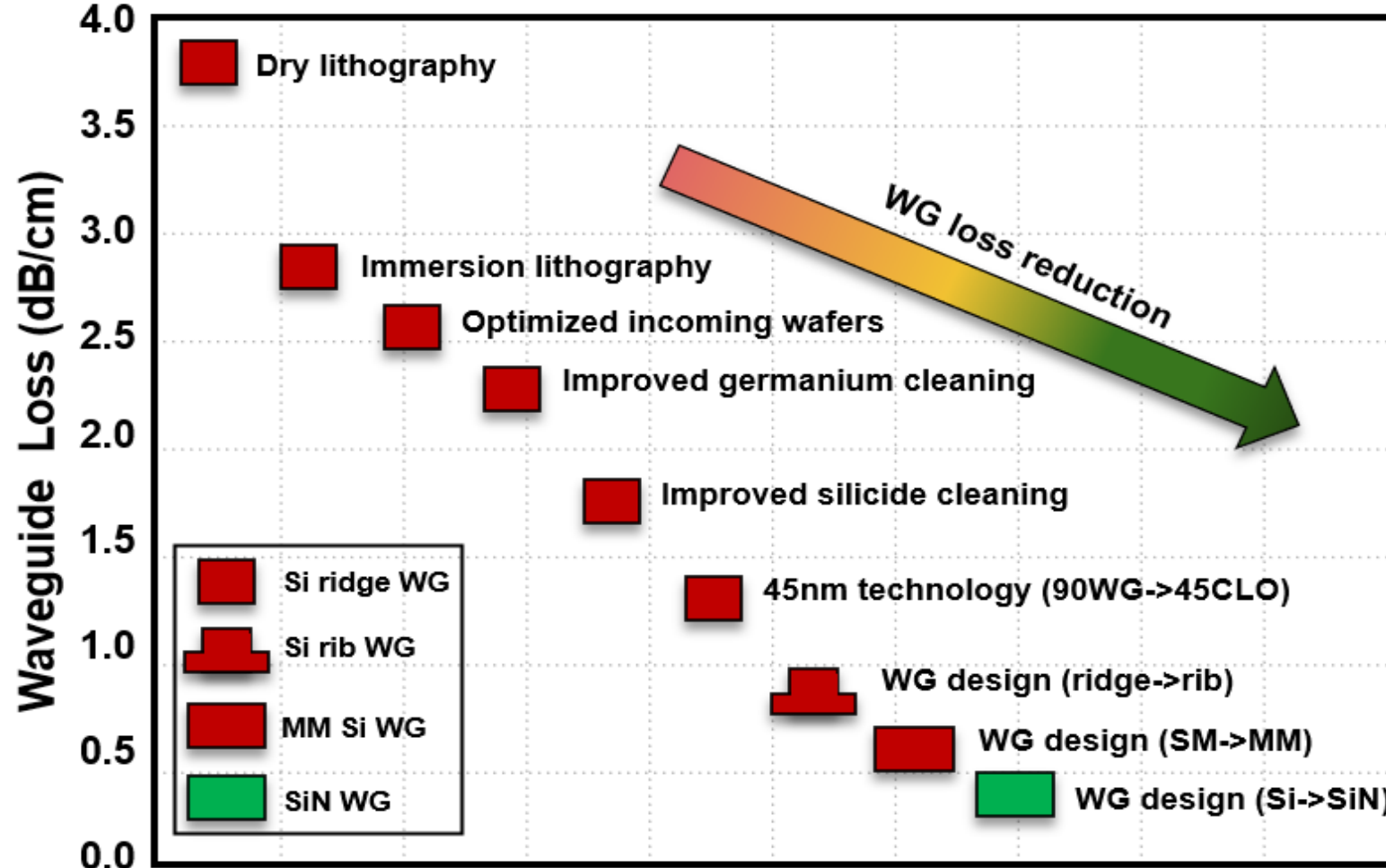
- ❑ Edge couplers and Advanced Packaging

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Waveguides on GF Fotonix™ platform: Loss reduction



Reference

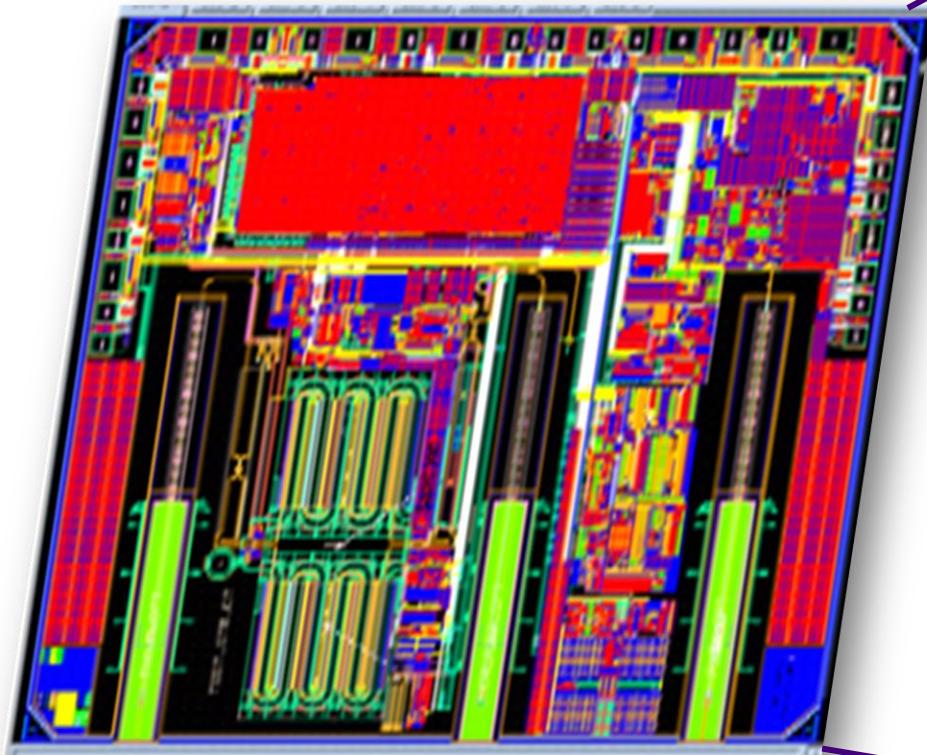
Y. Bian, et al., OSA FiO, FW5D.2 (2020).

Y. Bian et al., OFC, Th1A.46 (2021).

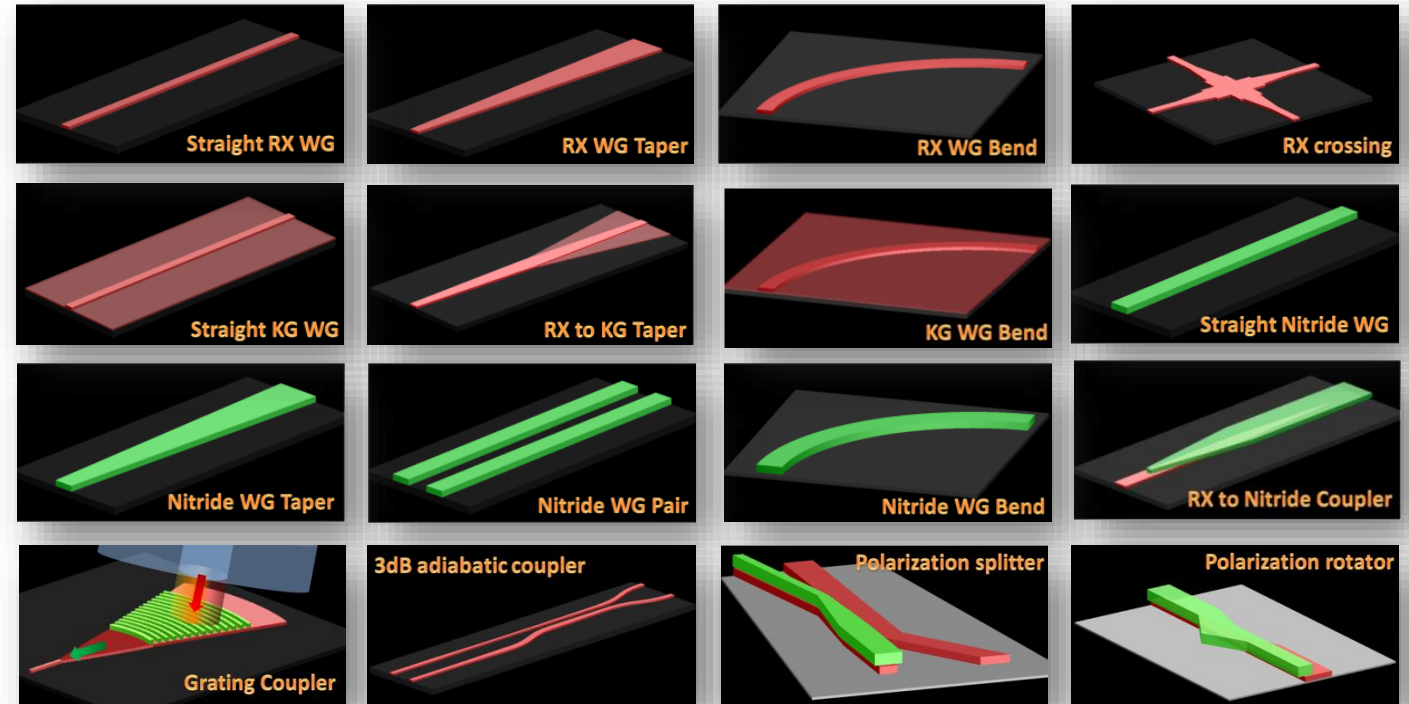
- **1.0 dB/cm reduction** - Immersion lithography
- **0.3 dB/cm reduction** - Optimized incoming wafer
- **0.2 dB/cm reduction** - Optimized germanium process
- **0.6 dB/cm reduction** - Optimized silicide cleaning process
- **0.45 dB/cm reduction** - Silicon ridge to rib waveguide
- **0.3 dB/cm reduction** - Single to multi-mode waveguide
- **0.8 dB/cm reduction** - Silicon to silicon nitride waveguide

Continue pushing the SiN WG loss below 0.1 dB/cm

GF Fotonix™ : Passive Library



Passive photonic building blocks on Si & SiN platforms

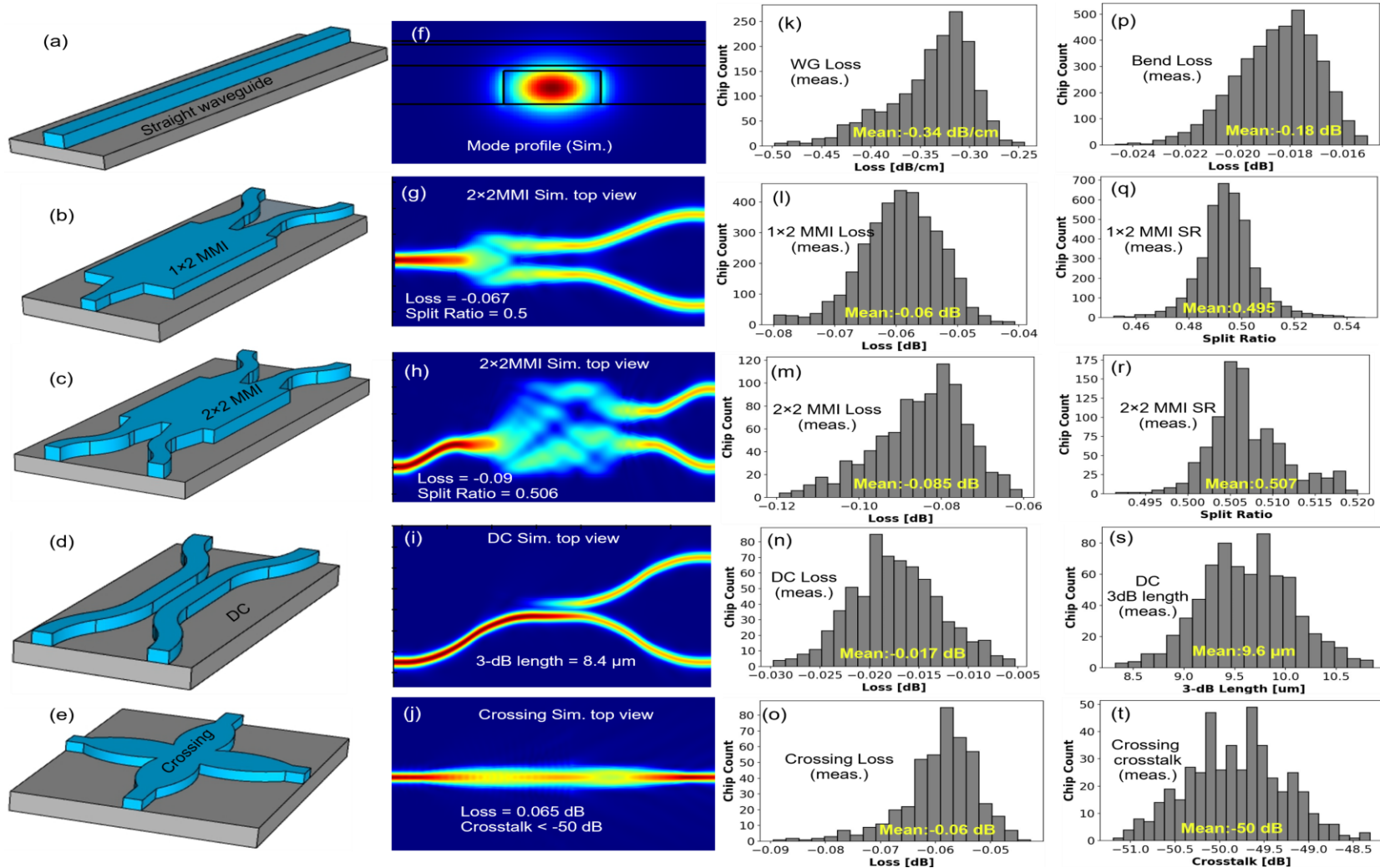


- Routing, coupling, polarization handling, wavelength filtering, etc.
- Si and SiN-based components covering O-band operation
- SM SOI Ridge (-1.0 dB/cm), SOI Rib (0.73dB/cm), SM SiN (0.39 dB/cm)

Reference

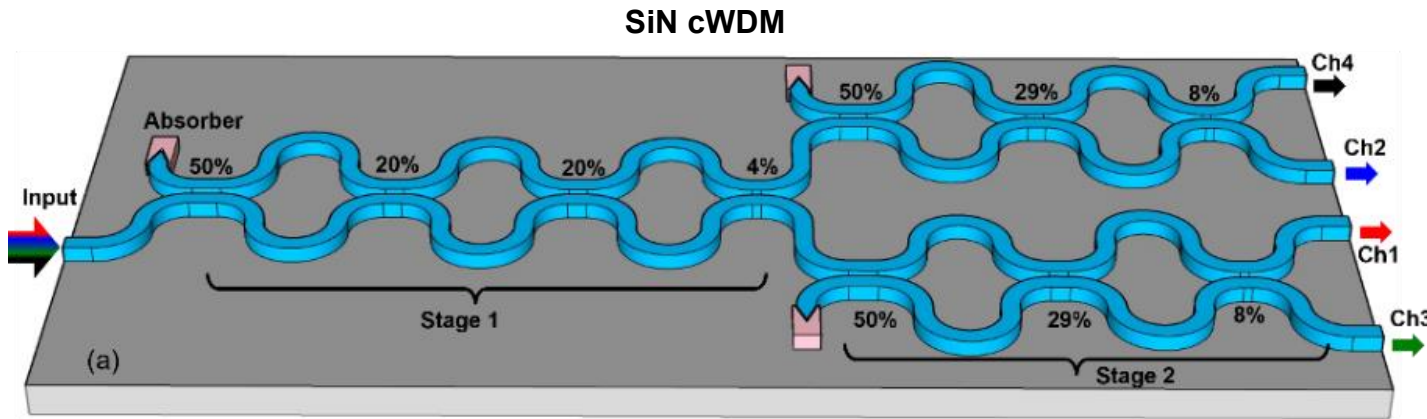
K. Giewont, et al., *IEEE JSTQE*, 25(5) 1-11 (2019).
Y. Bian, et al., *OSA FIO, FW5D.2* (2020).
M. Rakowski, *OFC T3H*. 3 (2020).

GF Fotonix™ : High-power SiN primitives



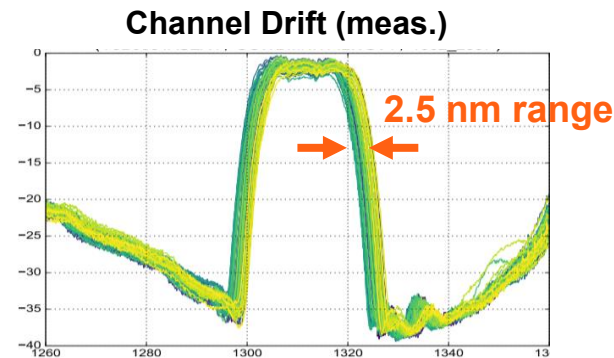
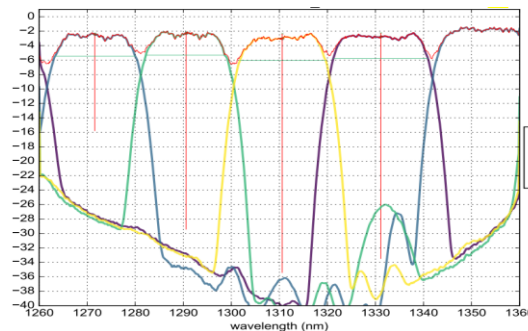
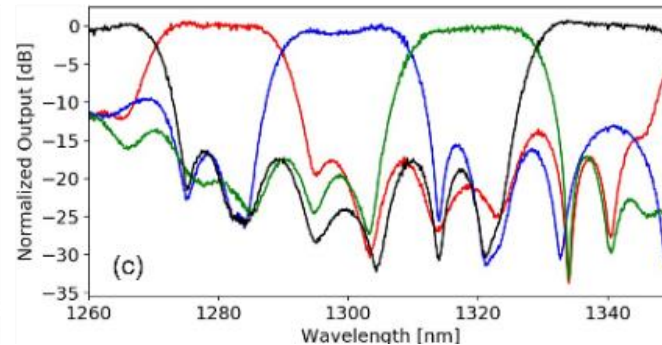
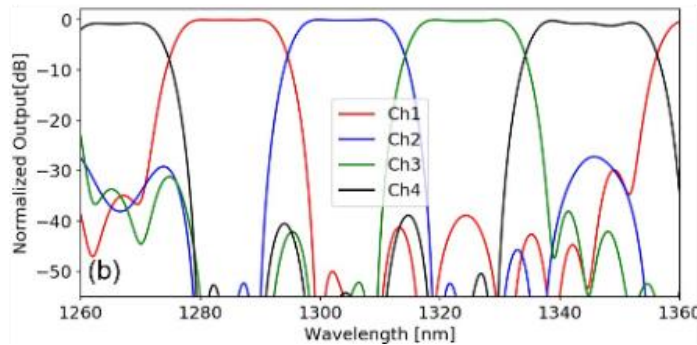
- ❑ Enhanced SiN suite to meet high power and high bandwidth requirements
- ❑ SiN primitives:
 - WGs and bends
 - 1X2 MMI and 2X2 MMI splitters
 - Directional couplers and taps
 - Crossings

Monolithic SiN cWDM



Simulation

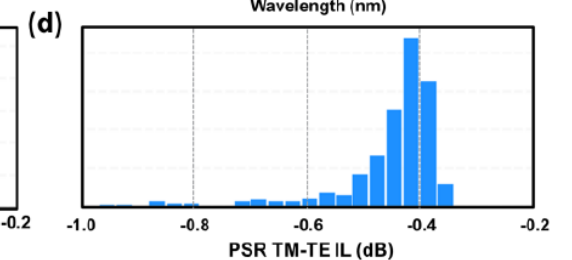
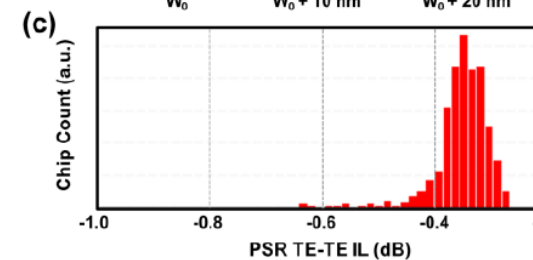
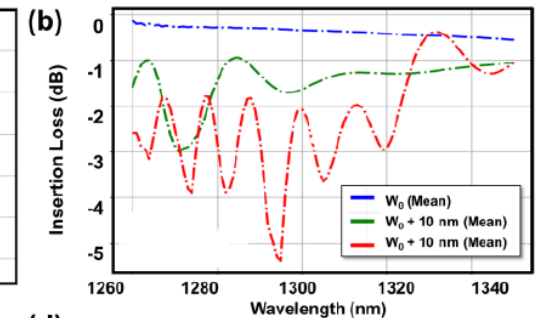
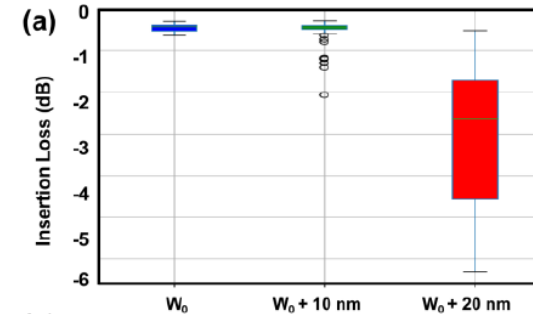
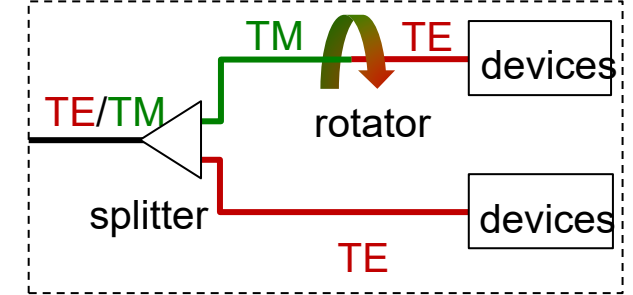
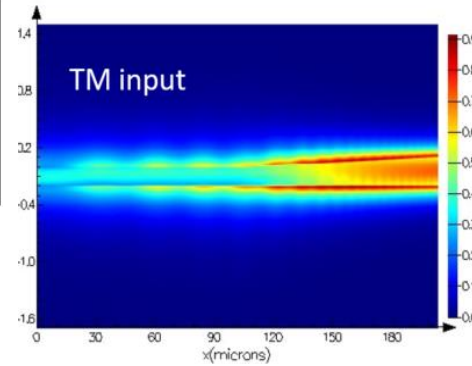
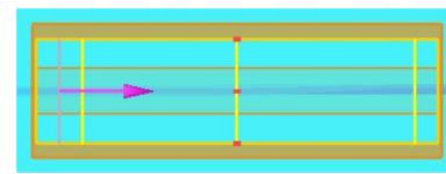
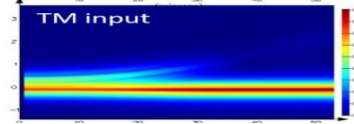
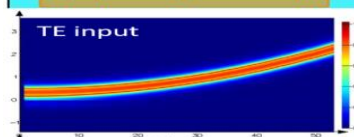
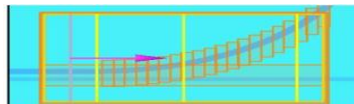
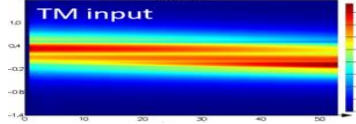
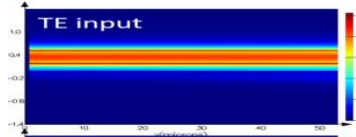
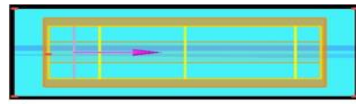
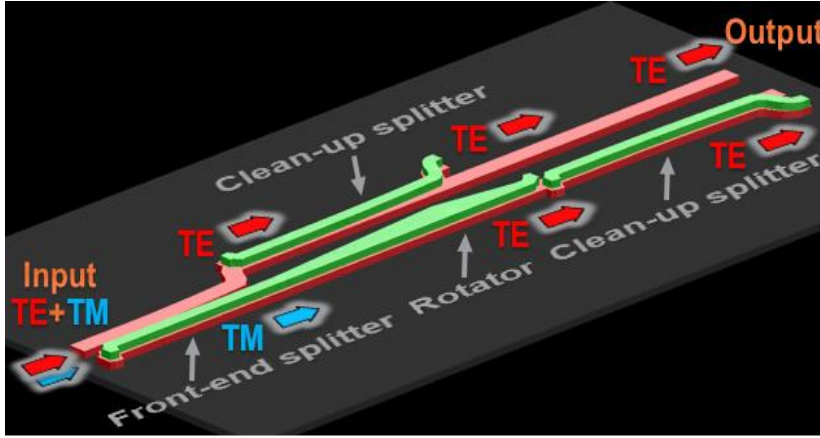
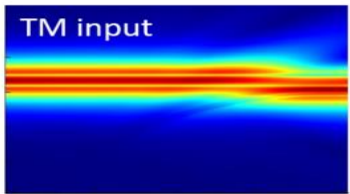
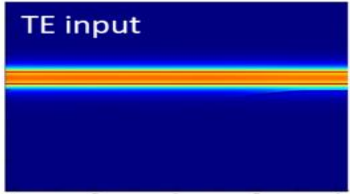
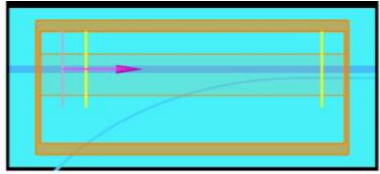
Measurement



SiN cWDM:

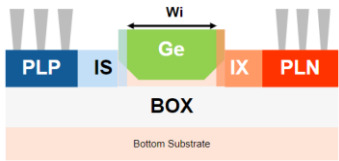
- Athermal WDM filter based on cascaded MZIs
- Proof-of-concept demonstration using monolithic SiN primitives
- 2 stage designs achieving 4 channels with flat-top response
- Continued design and process optimization to meet IEEE/MSA cWDM standards and enhance the performance
 - Delay length optimization to adjust the channel center
 - Clean-up filter to further reduce the crosstalk
- Through recent advances in film deposition and patterning, GF has realized **2.5 nm channel drift** across a full 300 mm wafer map.

On-chip polarization management: PSR

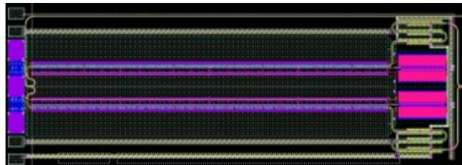
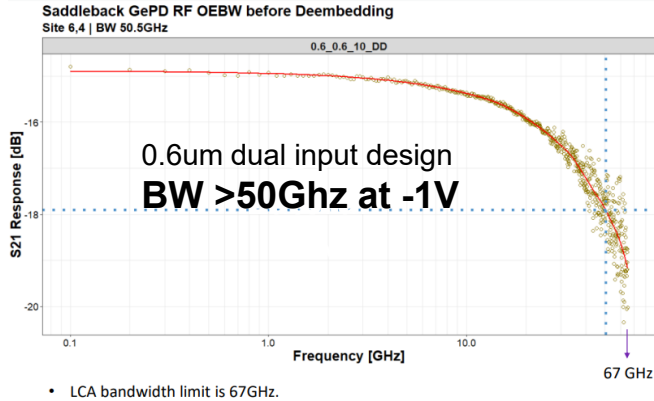


- High performance, broadband monolithically integrated polarization splitter and rotator using Si and SiN layers
 - Low IL < 0.42dB, low PDL: <0.1 dB @ 1310 nm
 - Low crosstalk < -45 dB
 - Footprint can be reduced with cross talk trade-off

GF Fotonix™ High Performance Active Photonic Devices



Ge PD >55GHz BW

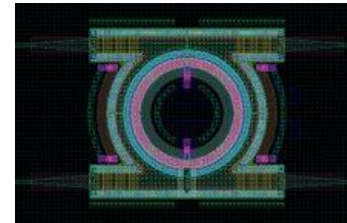


MZM: 53Gbaud PAM4

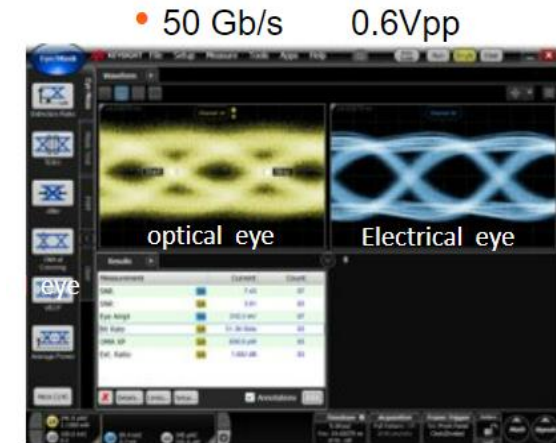
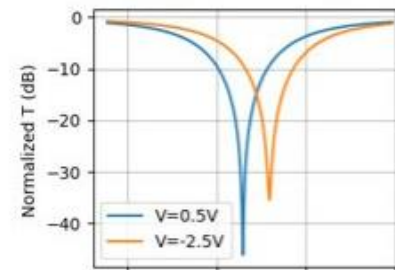
53 GBd PAM4 (-1 Vbias, 3.2 Vppd)



- ❑ High performance active photonic device library:
 - >55 GHz Germanium photodetectors
 - >35 GHz MZI and ring modulators
- ❑ **Next generation** active devices under development:
 - Targeting **> 60 GHz E-O/O-E BW**



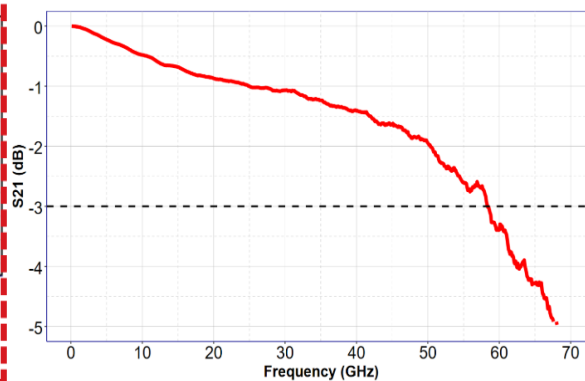
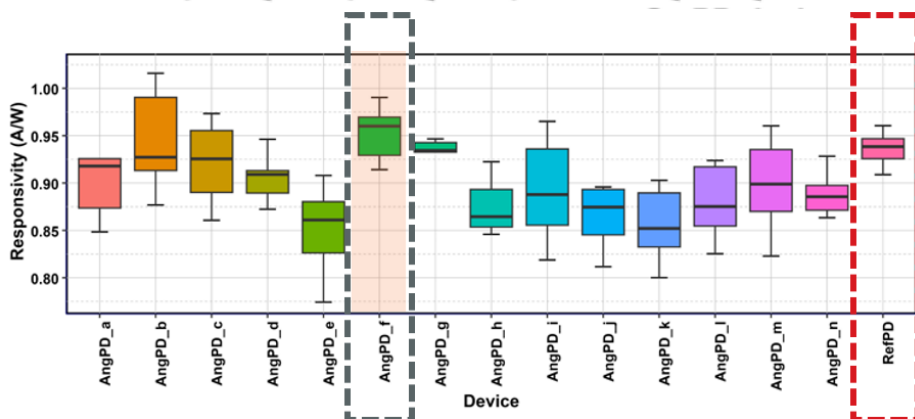
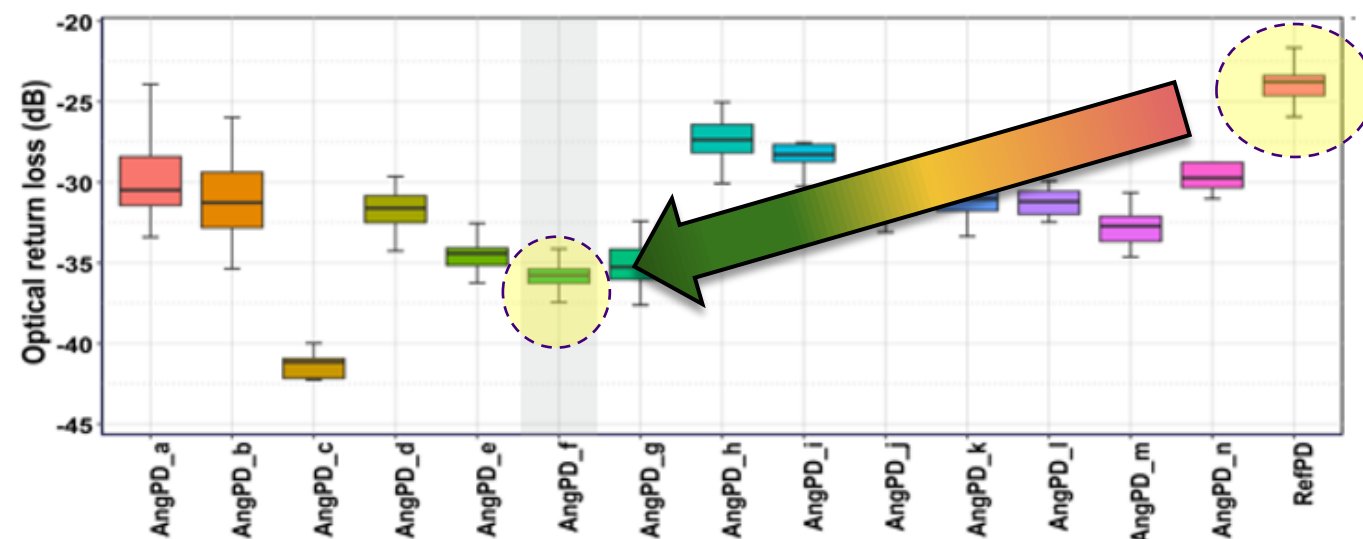
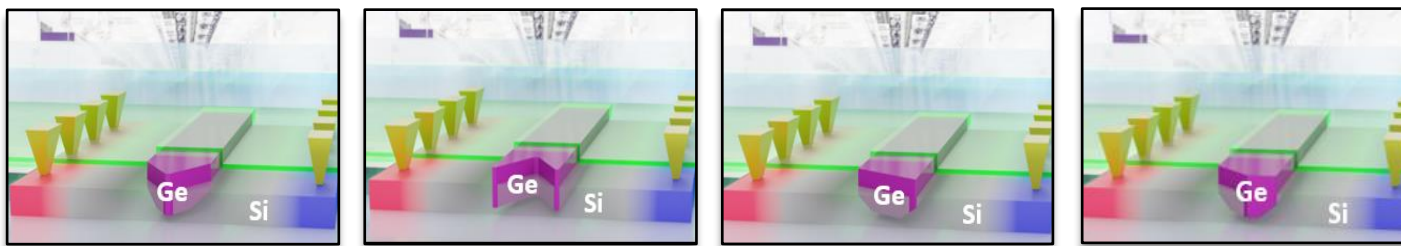
Ring modulators >35GHz BW



Reference

K. Giewont, et al., *IEEE JSTQE*, 25(5) 1-11 (2019).

Low reflection (ORL) Ge PD

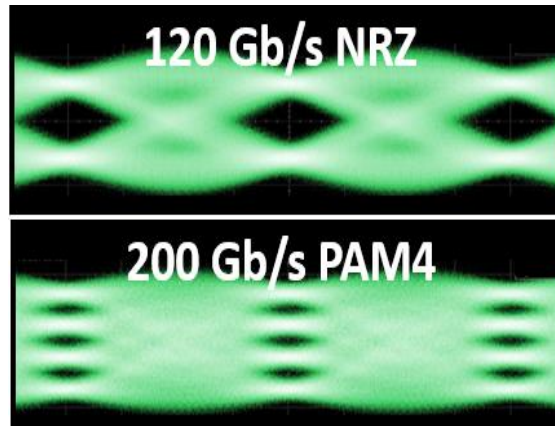
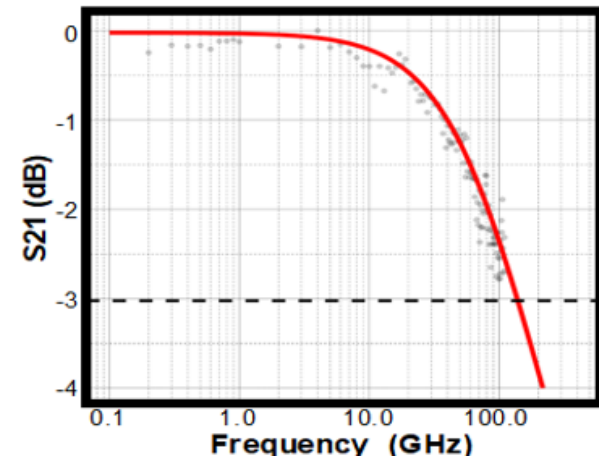
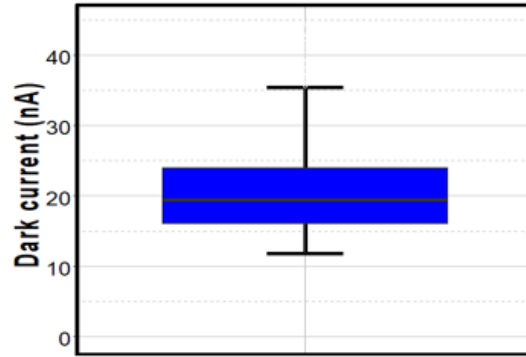
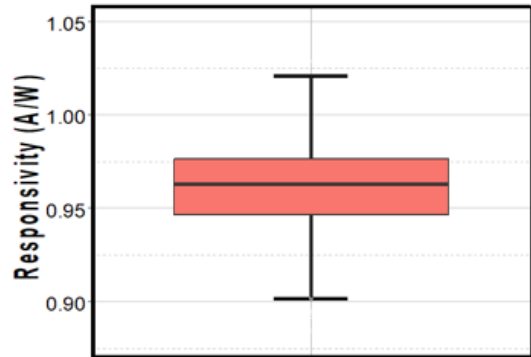
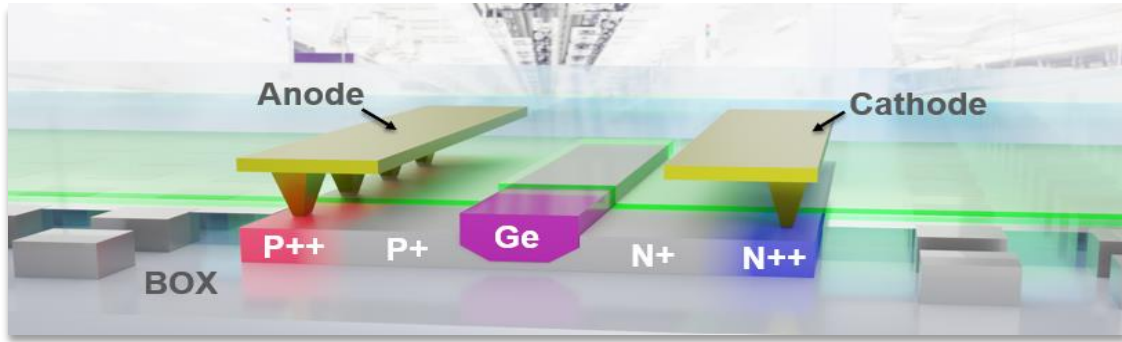


- Inaugural experimental demonstration of angled PD designs on 300-mm monolithic CMOS-SiPh platform for ORL reduction
- Ultra-low ORL of **<-36 dB** @ 1310 nm
 - vs **-23 dB** in POR rectangular PD
- Excellent DC/AC performance
 - **>0.95 A/W** responsivity
 - **<30 nA** median dark current
 - 3dB OE BW ~ **60 GHz**
- GlobalFoundries Fotonix™ offering ready for prototyping

ORL	Resp	Idark	BW
<-36 dB	>0.95 A/W	<30 nA	~ 60 GHz

Source: Y. Bian, Th3E.6, OFC2025

Ultra-fast high-power Ge PIN PD with record high BW-Resp Product



- Inaugural experimental demonstration of ultra-fast Ge PD designs on 300-mm monolithic CMOS-SiPh platform

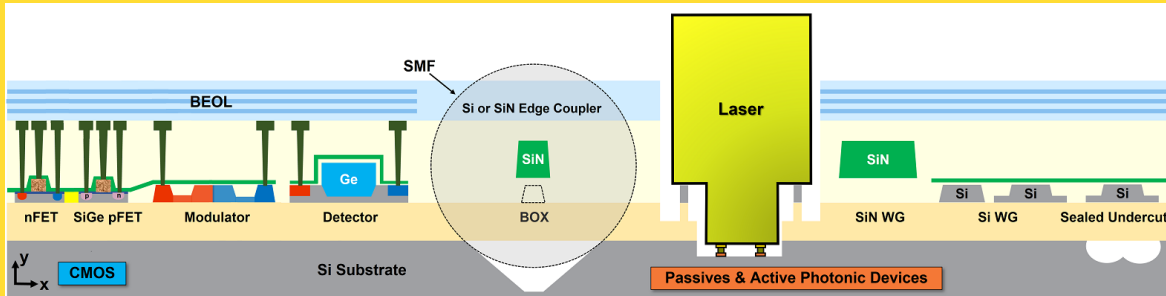
- **Record-high BW-Resp product > 130 GHz*A/W**
- **>135 GHz** OE bandwidth
- **>0.96 A/W** responsivity
- **<20 nA** median dark current
- **<-36 dB** optical return loss

- **Ongoing work**

- Monolithic TIA integration
- Co-optimized device-circuit design > 400G
- BER testing
- Reliability assessments under extended temperatures

Source: Y. Bian, Postdeadline paper V, CLEO 2025

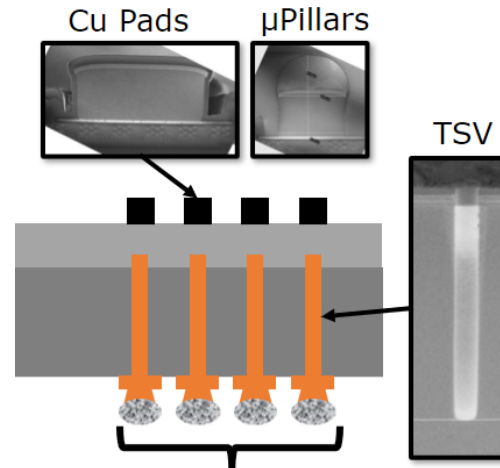
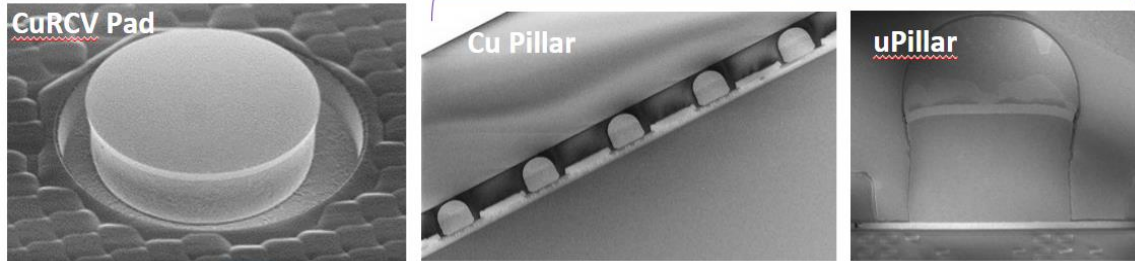
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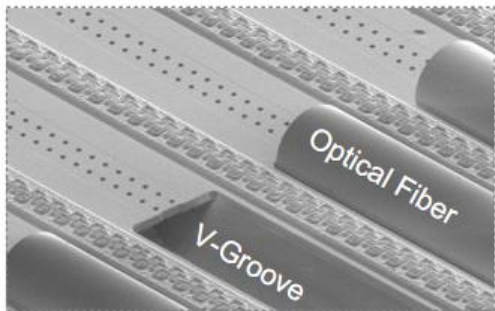
Advanced Packaging Features

**Cu pillar and Cu pillar receive
100-150um pitch w/ 55um pitch in development**

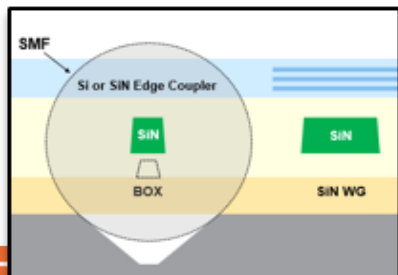


**TSV with Cu Pillar
to enable 2.5D and
3D packaging**

Tighter pitch for high-speed
electrical interface e.g. UCIE

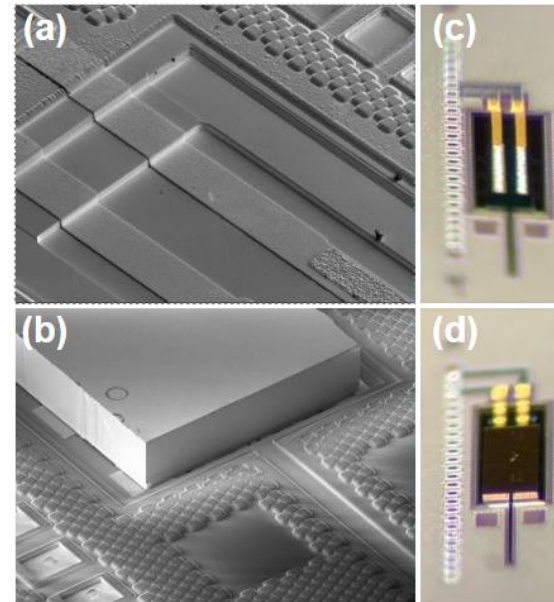


**Passive Vgroove fiber
attach. SOI and high-
power SiN couplers.
250 to 127um pitch
& Pluggable I/O**



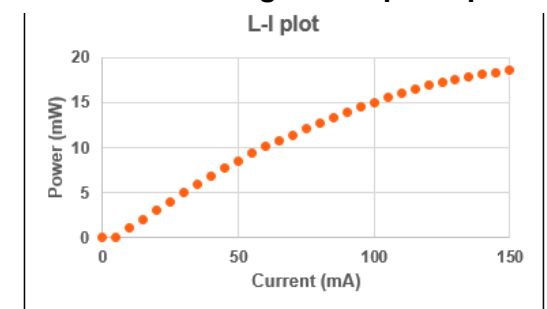
SiN Vgroove measured results (nominal)

	TE	TM
IL (dB)	<0.6	<0.8
ORL (dB)	<-39	<-39
Optical pwr (mW)	>520	>520

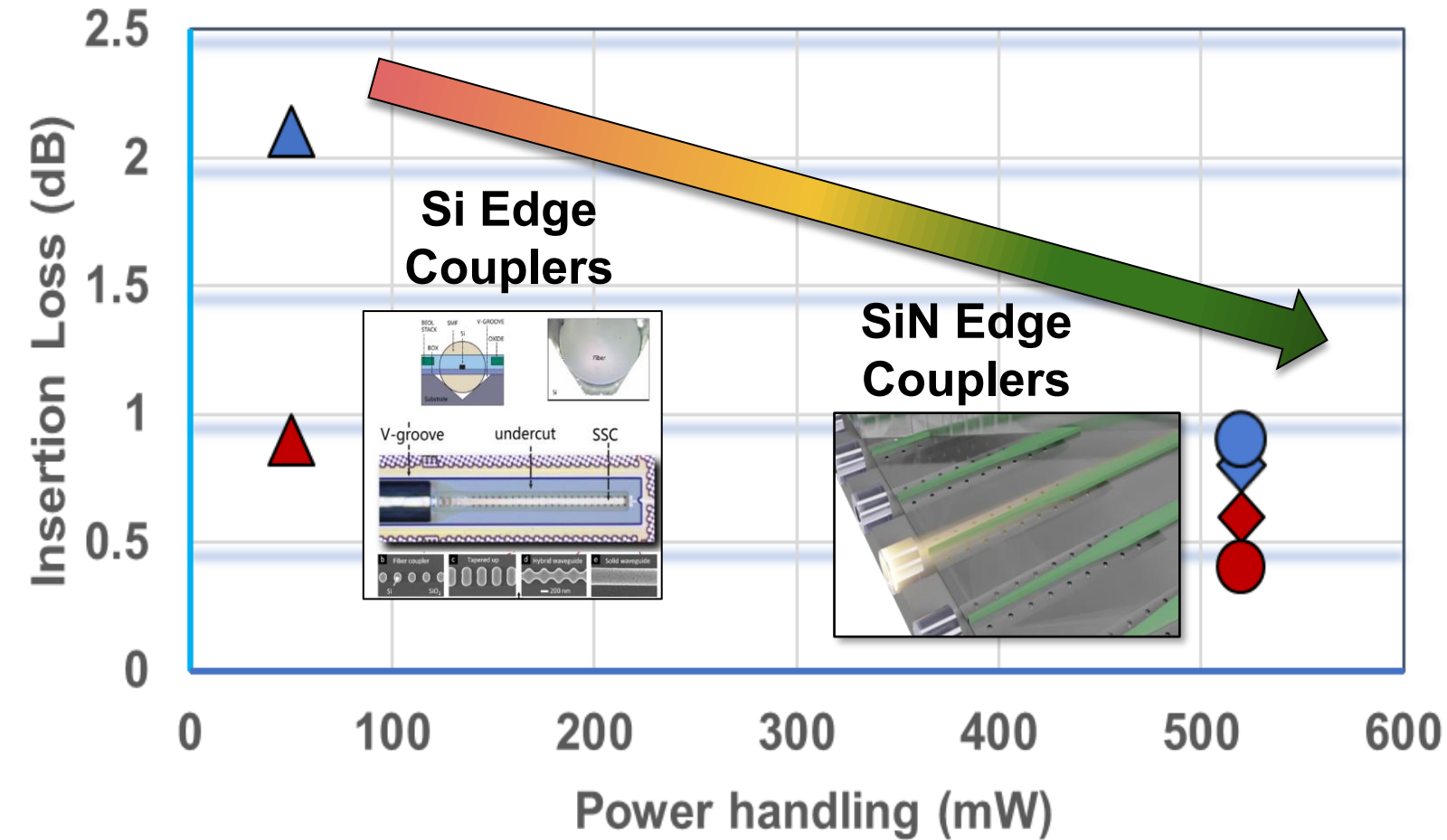


**Laser cavity to
enable direct hybrid
laser attach on PIC
in development**

L-I measured thru Vgroove optical path



Towards low-loss, high power, self-aligned fiber attach solution

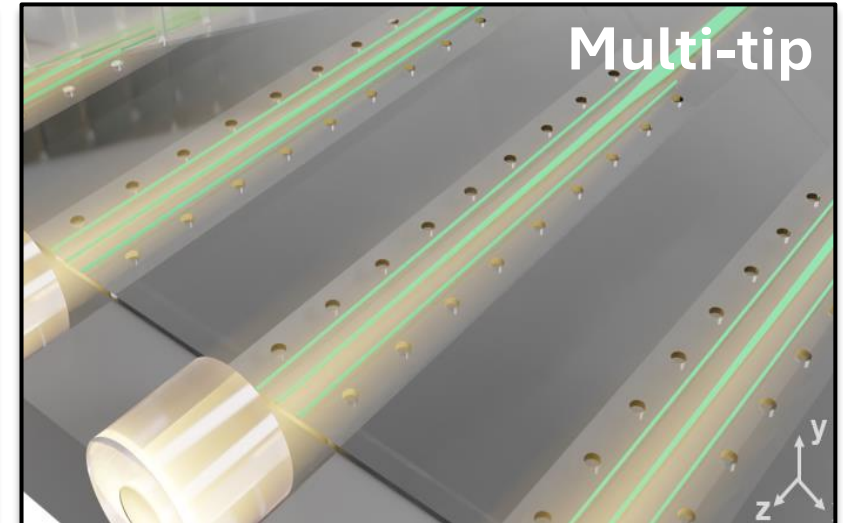
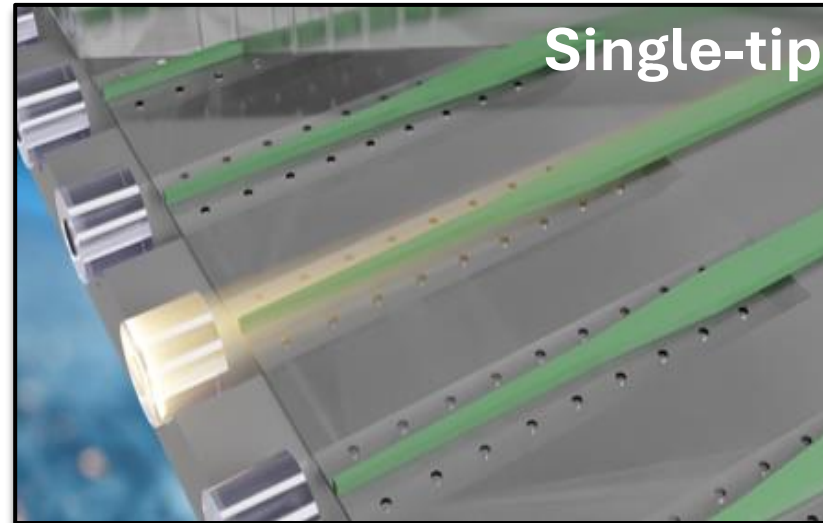
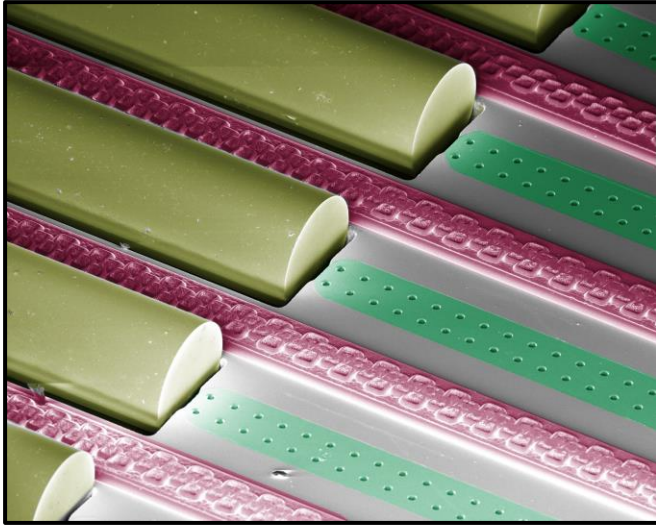


- ❑ **Need for high-performance fiber attach:**
 - High transmission efficiency (**< 1 dB**)
 - Low polarization dependent loss (TE vs TM) **< 0.5 dB**
 - Low back reflection (IEEE 802.3cu-2021: **ORL < -26 dB** for overall TX or RX)
 - Broadband operation (e.g. O-band, C-band)
 - **High power handling (e.g. > 100 mW)**
 - Self alignment (e.g. V-groove)

- ❑ **Solution:** switching from **Si edge coupler** to **SiN edge coupler**

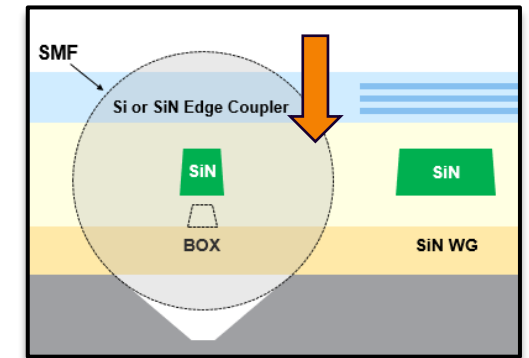
Source: Y. Bian, et al., OFC M3C.3 (2023); Y. Bian, et al., CLEO AA129.1 (2025)

Monolithically integrated SiN edge couplers (single/multi-tip)



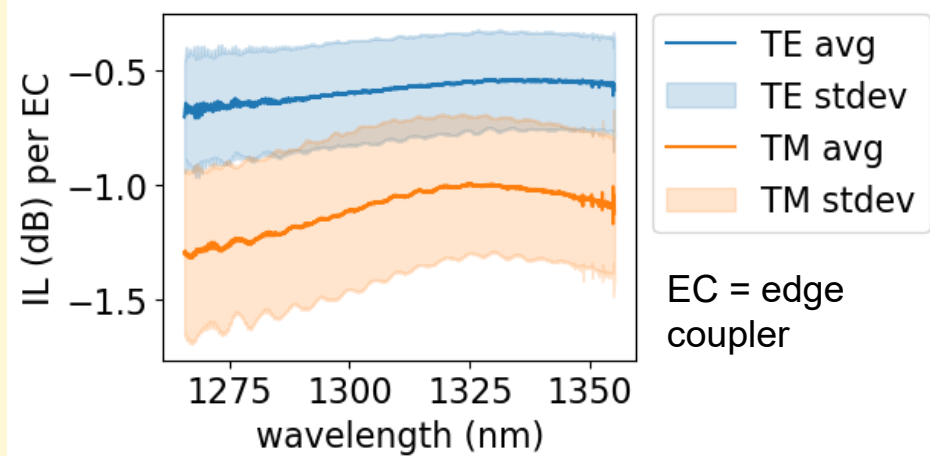
❑ Integration of high-performance SiN edge coupler on the monolithic SiPh platform

- Leveraging existing MOL SiN waveguide layer which has good high power handling capability
- **193-nm DUV litho** and **advanced free-form OPC** ensuring high pattern fidelity and minimized loss
- Advanced **TMAH module** forming **V-groove** with **precisely controlled shape** and **dimensions**
- **Undercut below the spot size converter** (SSC) preventing optical leakage into the substrate
- BEOL replaced with **thick TEOS cladding** for improved mode matching with SMF
- Additional process optimizations **preventing SiN SSC from being damaged** during BEOL removal
- **Simultaneous integration of Si and SiN edge couplers** on the same monolithic PIC now becoming possible
- SSC geometry and shape optimization enabling **improved mode matching** and **reduced conversion loss**

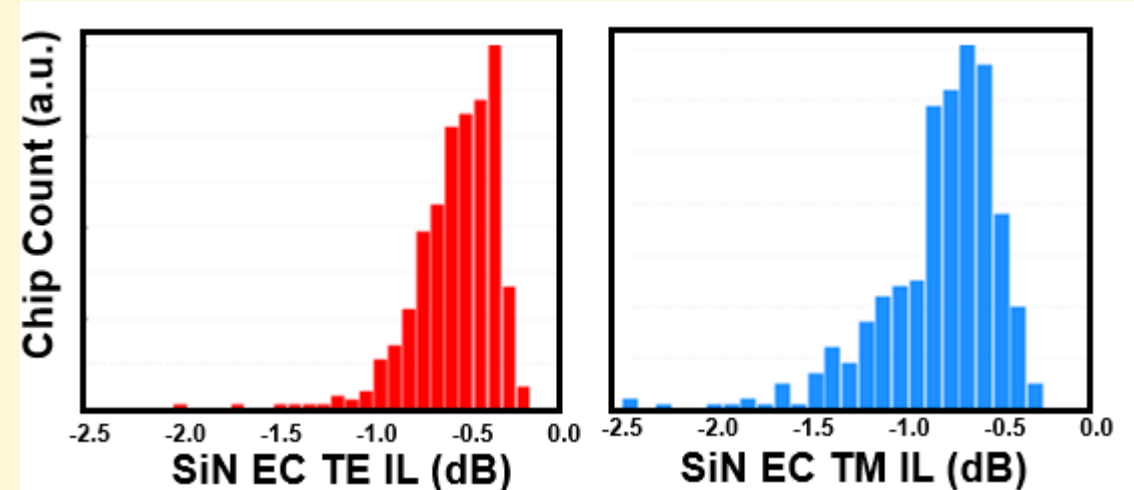


16-channel 250 μm -pitch SiN EC with low IL and flat through-band loss

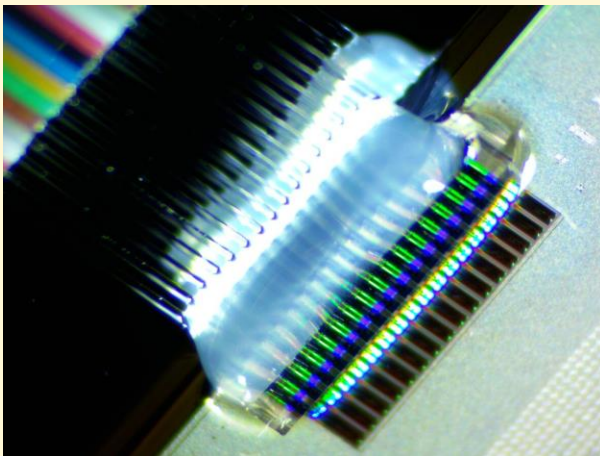
Flat wavelength response across large sample size



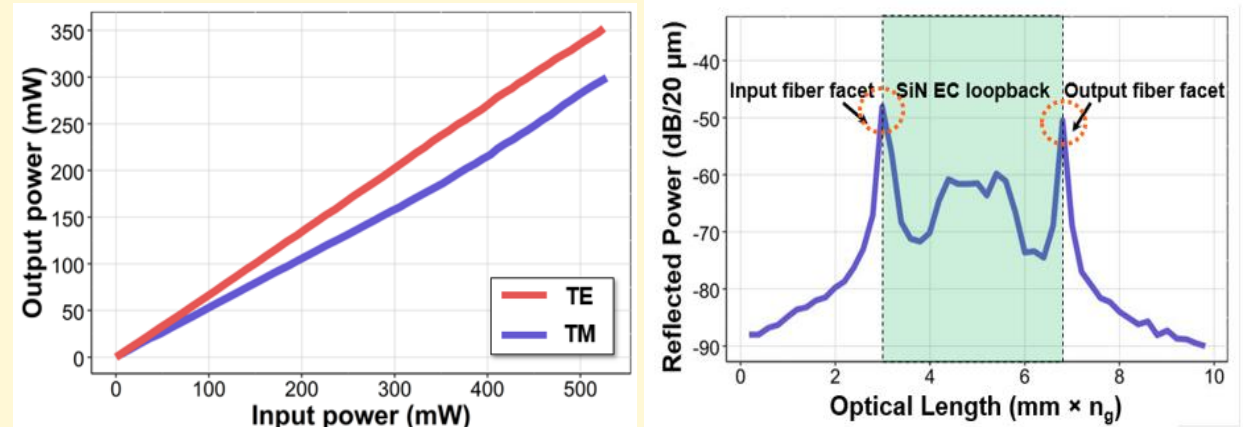
Large sample size of passive fiber attach shows low average IL



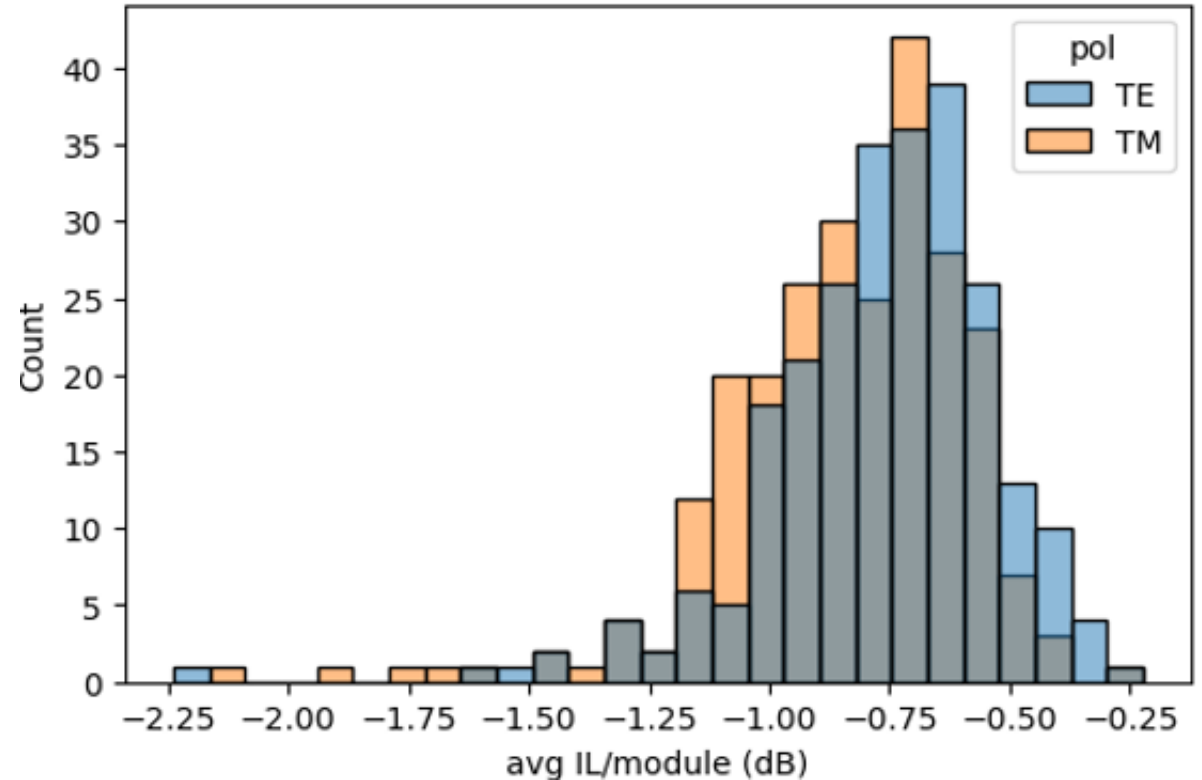
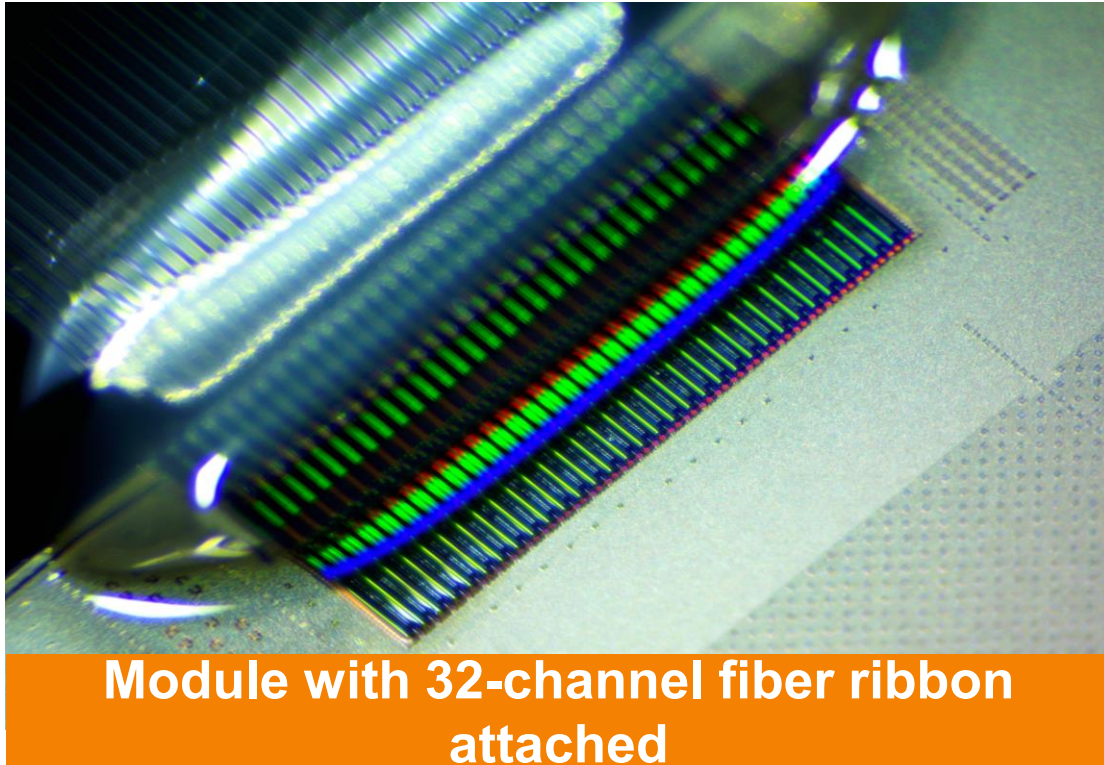
16-channel 250 μm pitch passive fiber attached to 16-channel V-groove array



High-power ramps continue show no roll-off in insertion loss up to 520 mW

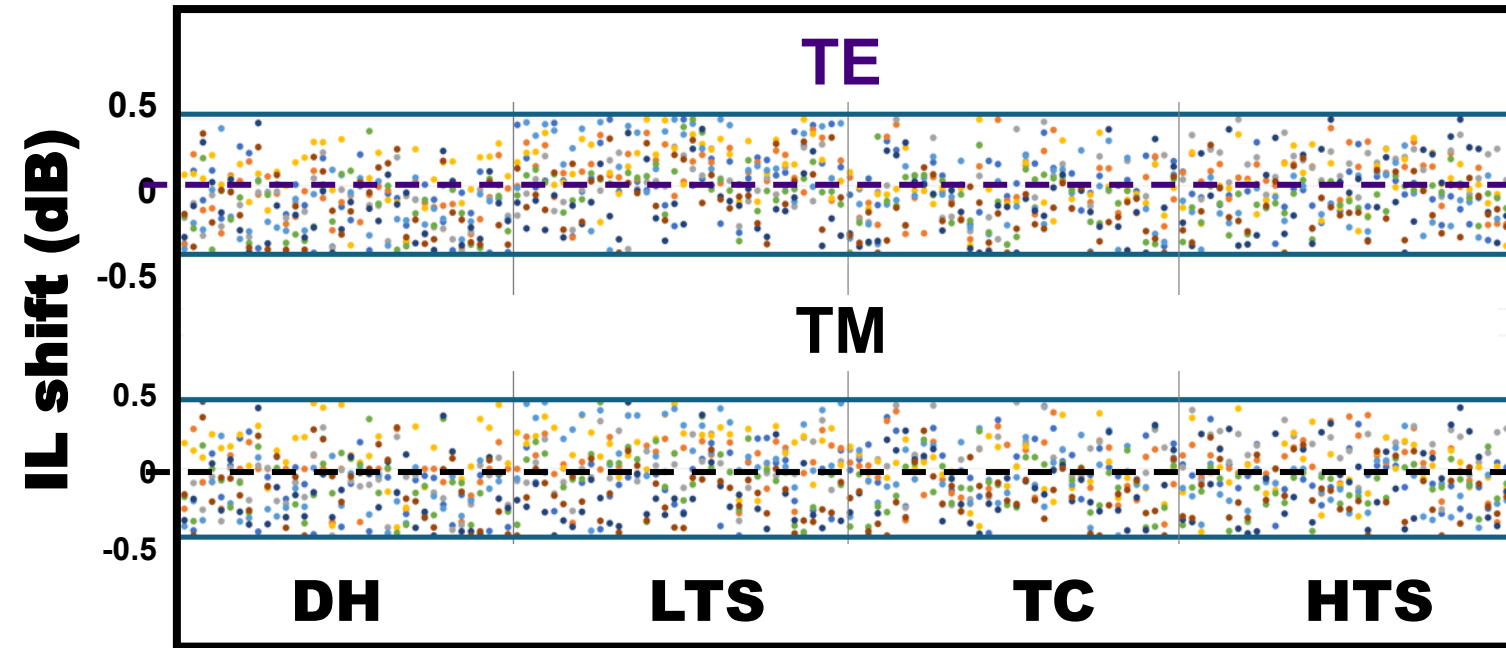


32-channel 127 μ m-pitch SiN EC with low IL/PDL/through-band performance



- Sub-1 dB TE and TM IL and < 0.1 dB PDL demonstrated on 32-channel 127 μ m-pitch Vgroove array, occupying the same footprint as a 16-channel 250 μ m-pitch array
- 2X Edge bandwidth/beachfront density by doubling the physical port count

127-um pitch SiN edge coupler full reliability assessment



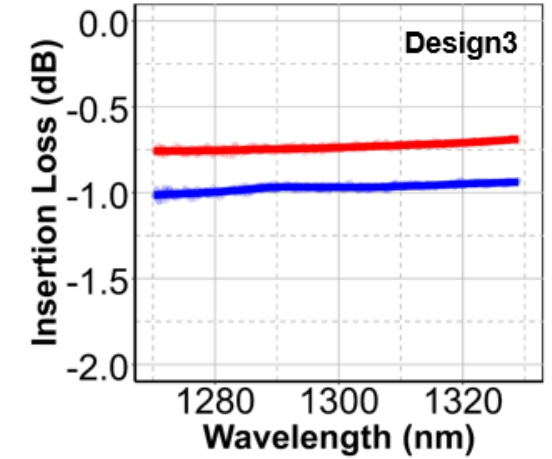
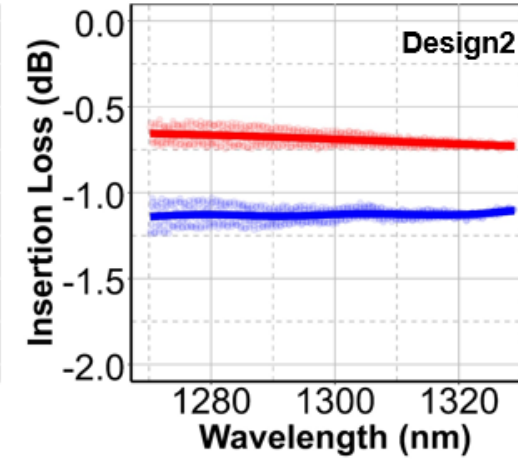
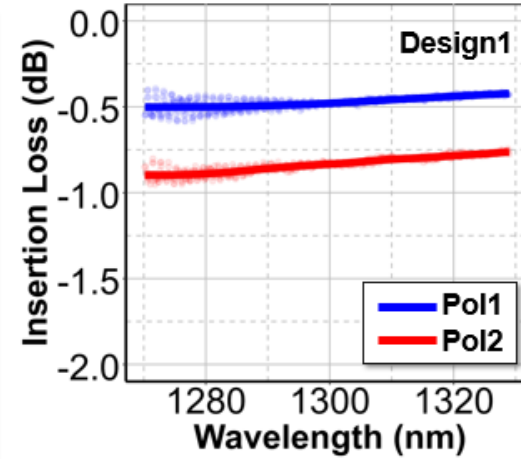
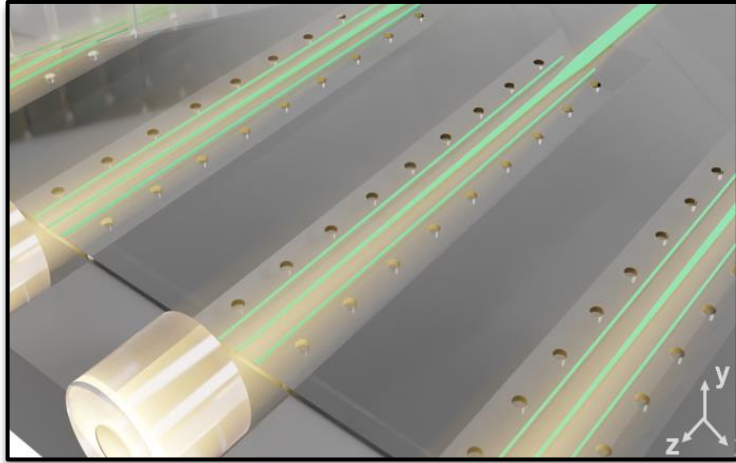
Test item (36 modules)	Result
LTS (-40°C, 72hrs)	Pass
HTS (105°C, 2000 hrs)	Pass
TC (-40°C to 105°C, 500 cycles)	Pass
DH (85°C/85% RH, 500 hrs)	Pass

□ SiN edge coupler module (127-um pitch) passed full reliability assessments

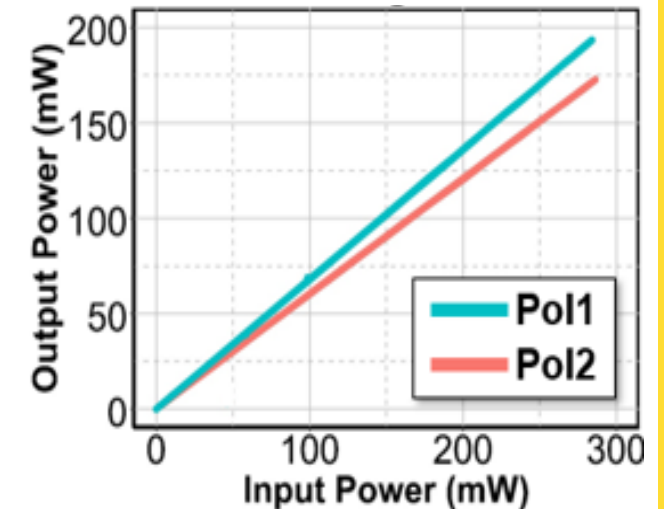
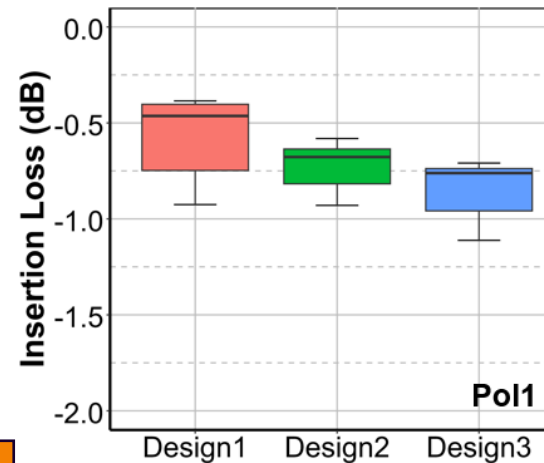
- Chip-fiber-package (CFP) qualification leveraging 36 modules
- Extensive reliability tests exceeding Telcordia specification GR-468 requirements
- IL delta **< 0.5 dB** for both polarizations before and after reliability test – indicating no obvious systematic degradation mechanism.

LTS: Low Temperature Storage
HTS: High Temperature Storage
TC: Temperature Cycling
DH: Damp Heat

Multi-tip SiN edge coupler for further IL reduction

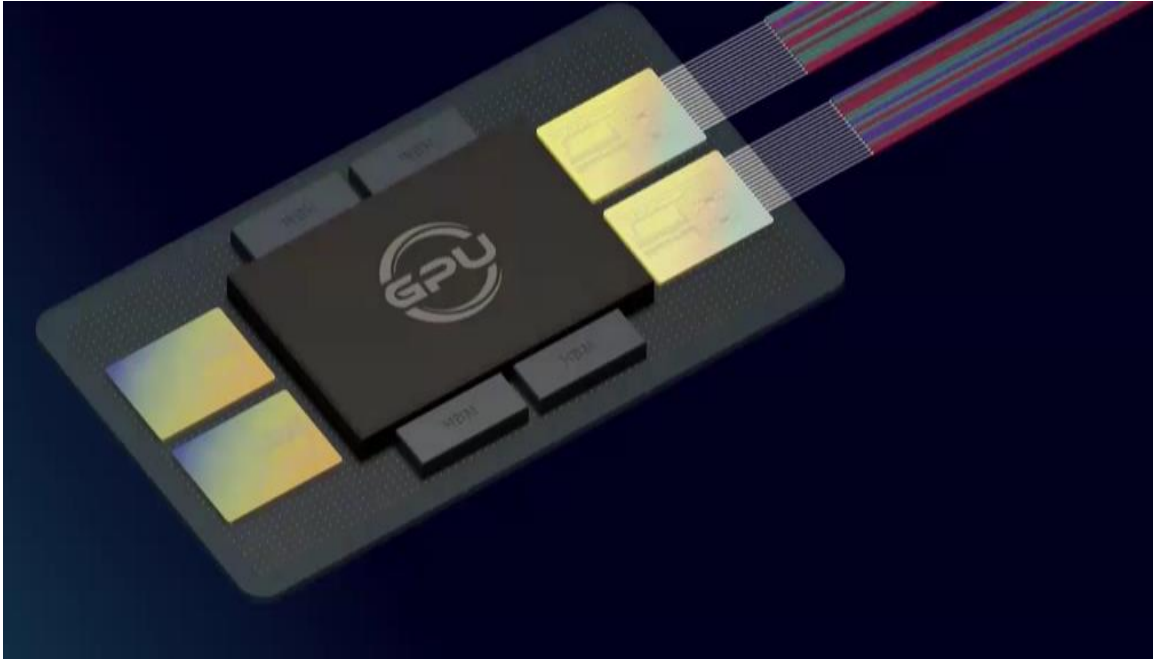


- ❑ Broadband high-power V-groove based multi-tip SiN edge coupler
 - **Lowest insertion loss reported: ~0.4 dB**
 - Low polarization dependent loss: **< 0.25 dB**
 - Low wavelength dependence: **< 0.2 dB**
 - Low optical return loss: **< -40 dB**
 - Good high-power handling: **expect > 520 mW**



IL as low as 0.4 dB @ O-band – lowest reported on 300-mm monolithic SiPh platform

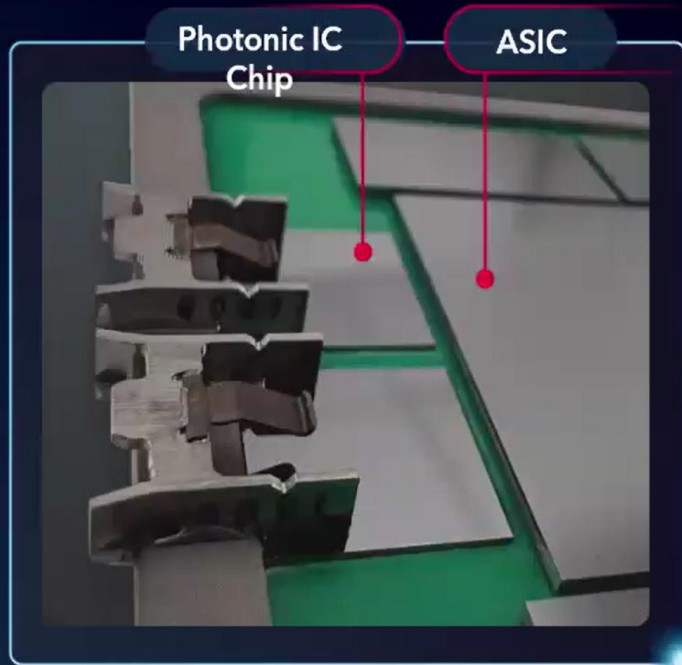
Fiber attach challenge for CPO & 2.5D integration



- ❑ Source: <https://teramount.com/>
- ❑ H. Taha, Scalable Detachable Fiber Connectivity for Seamless Integration With Advanced Semiconductor Packaging, OFC, W4A.3 (2025).

Challenges	Details
2.5D fiber integration	Photonics+Logic+HBM, Thinned PIC with TSV, reflow compatibility
Bandwidth scalability	Fiber counts, shoreline high density
Mechanics reliability	Form factor, mechanical stresses, warpage, fiber handling and routing
Thermal reliability	High temp, colling
Manufacturability	Reworkability, cleanness, testability
Ecosystem combability	Supply chain flow, foundry, cost

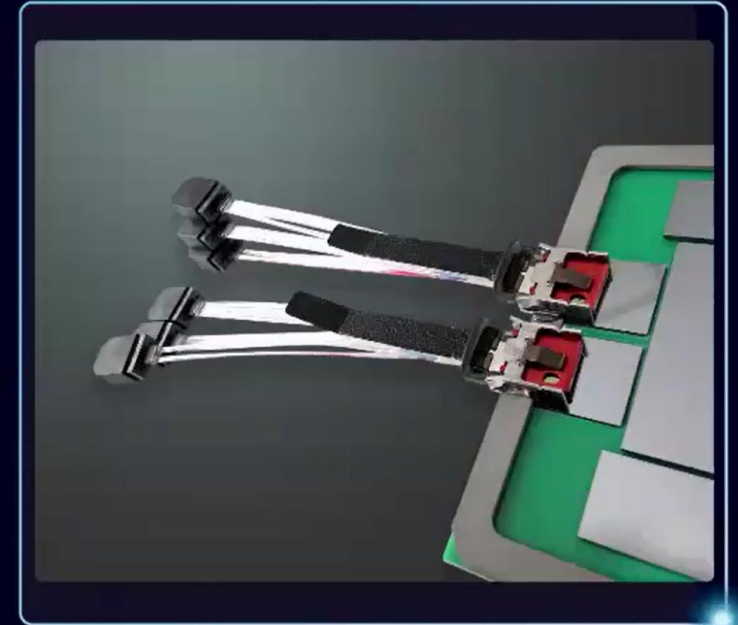
Teramount Detachable Fiber Connectivity Solution



2.5D Packaging Architectures



Detachable Fiber Connector,
10's Fibers, 127um pitch

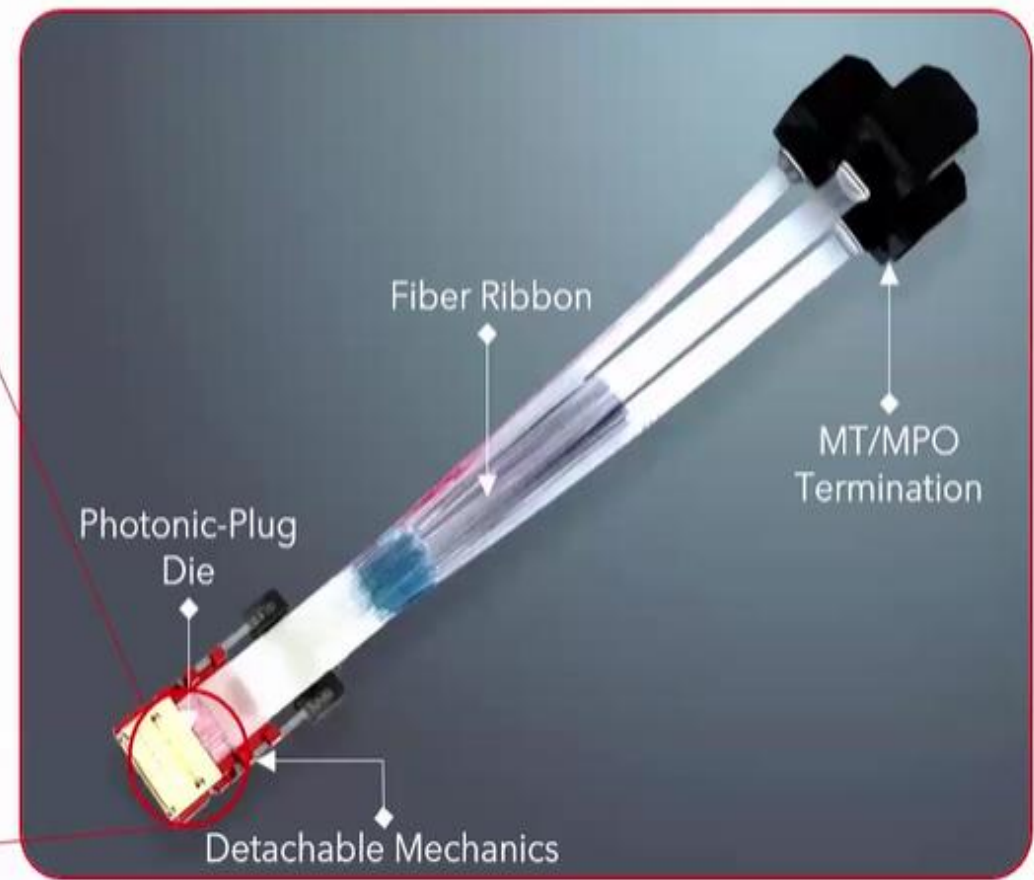
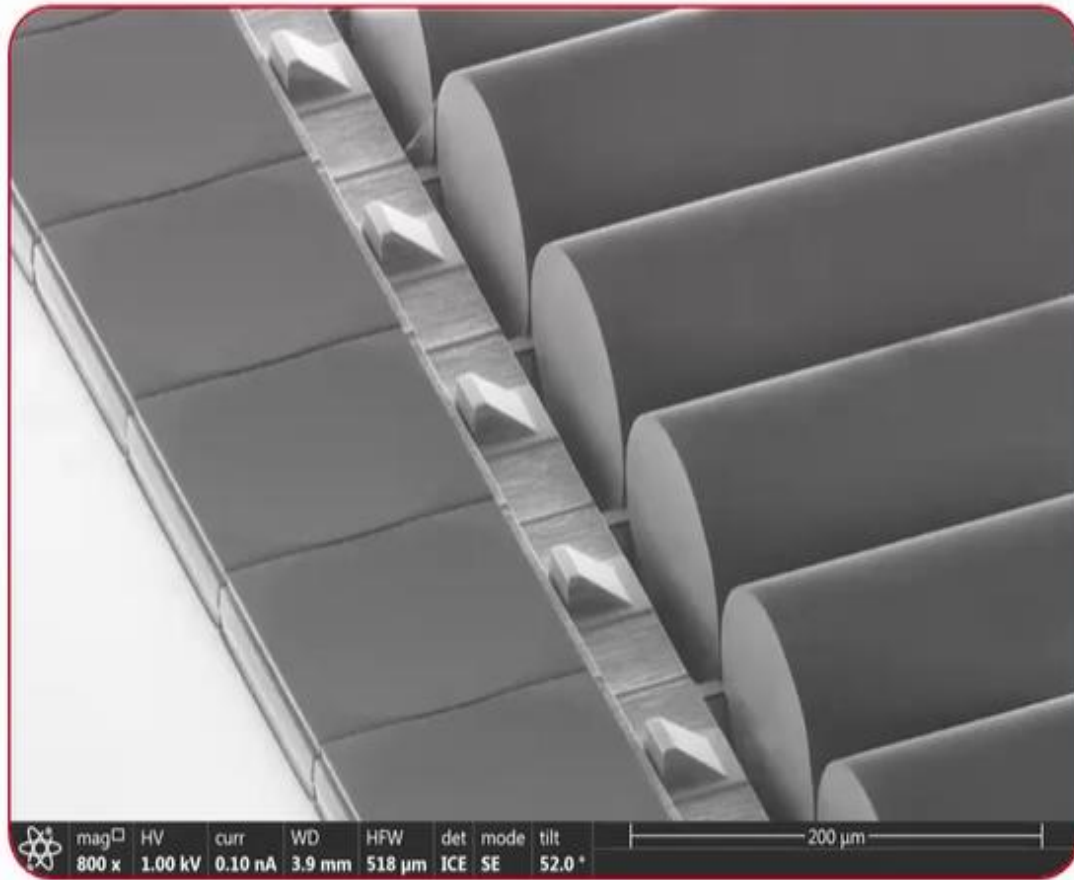


Large Fiber Count for Highest
Bandwidth Density

❑ Source: <https://teramount.com/>

❑ H. Taha, Scalable Detachable Fiber Connectivity for Seamless Integration With Advanced Semiconductor Packaging, OFC, W4A.3 (2025)

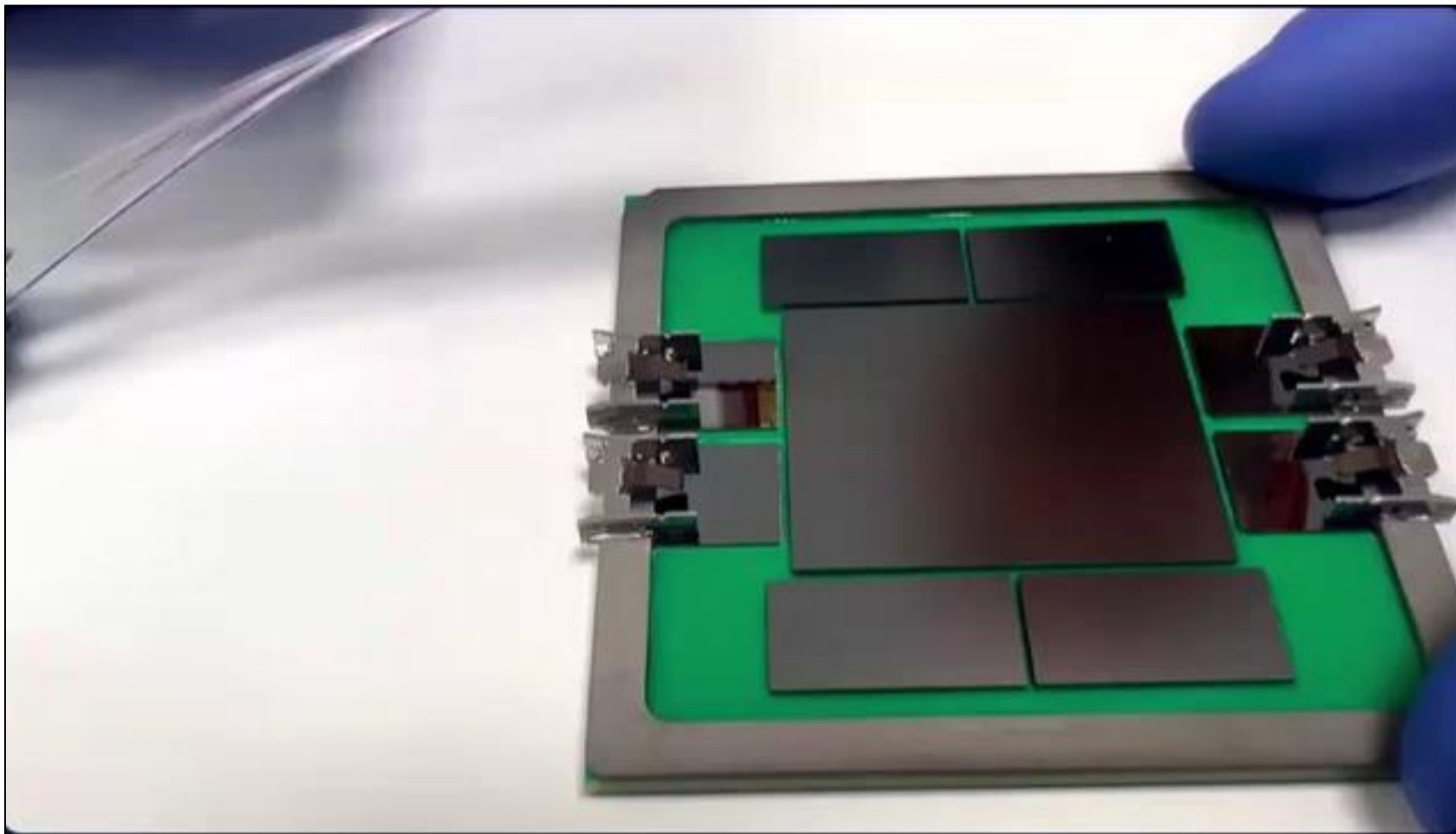
Photonic-Plug fiber connector



- ❑ Wafer level fabrication process enabling high accuracy photonic-plug interfacing with SMF/PMF
 - Large fiber account: 10's SMF/PMF

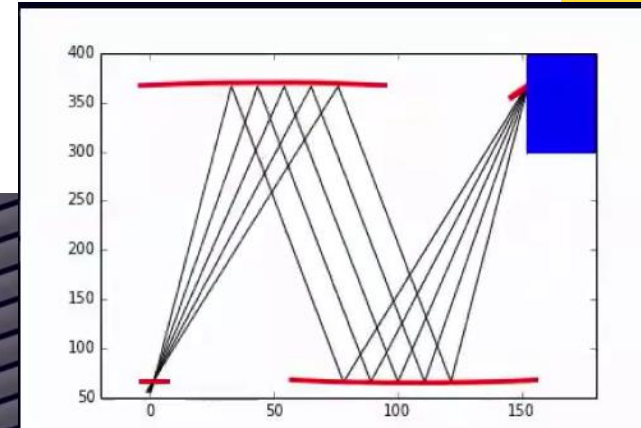
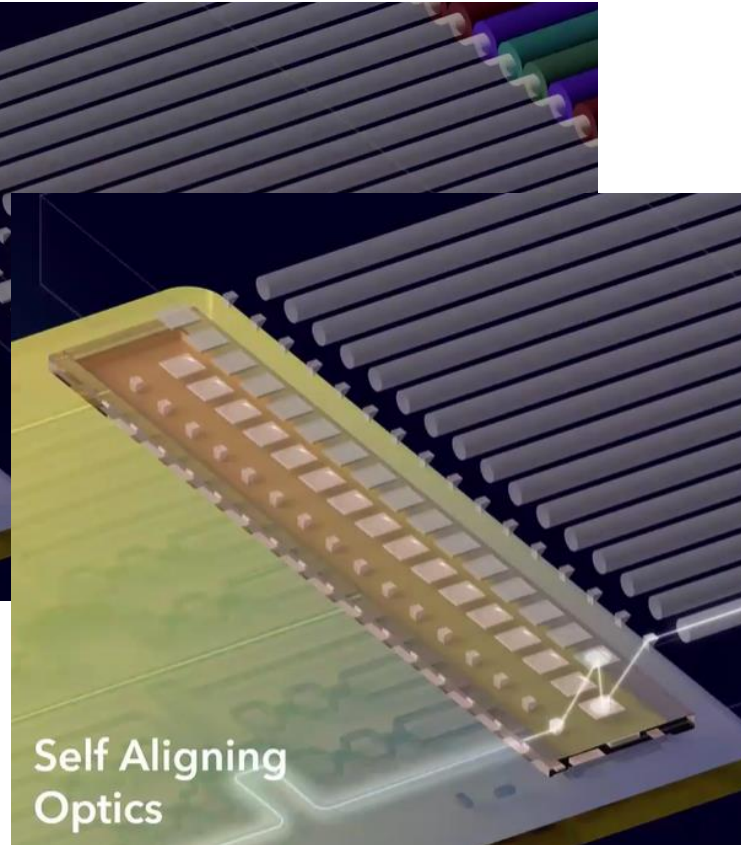
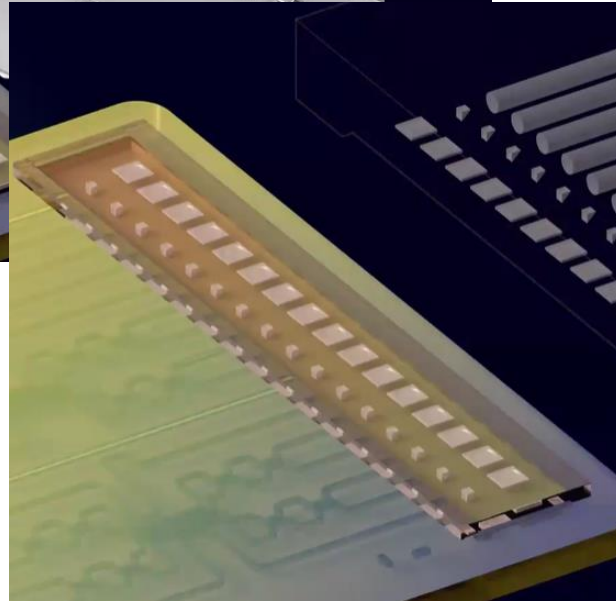
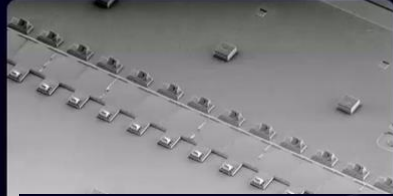
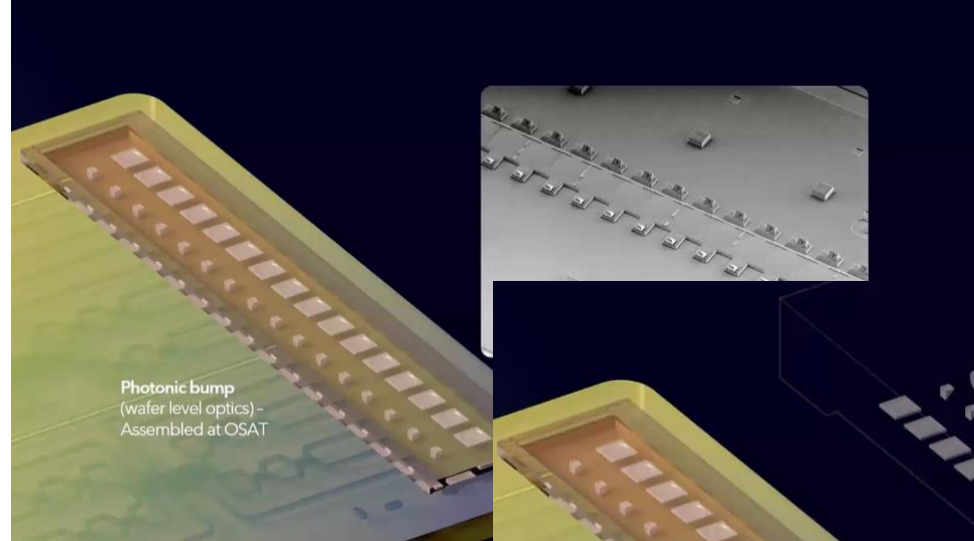
- ❑ Source: <https://teramount.com/>
- ❑ H. Taha, Scalable Detachable Fiber Connectivity for Seamless Integration With Advanced Semiconductor Packaging, OFC, W4A.3 (2025).

Photonic-Plug fiber connector

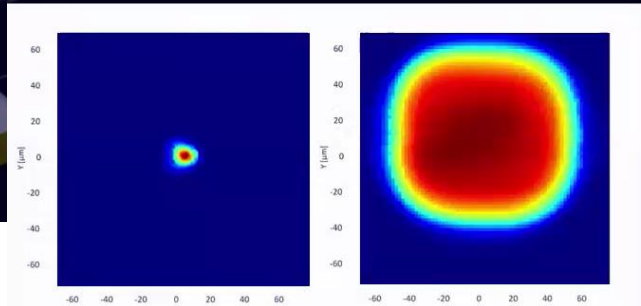


- ❑ Demo showing how the photonic plug fiber connector can be plugged and unplugged into a SiPh die which includes photonic circuits and mechanical elements

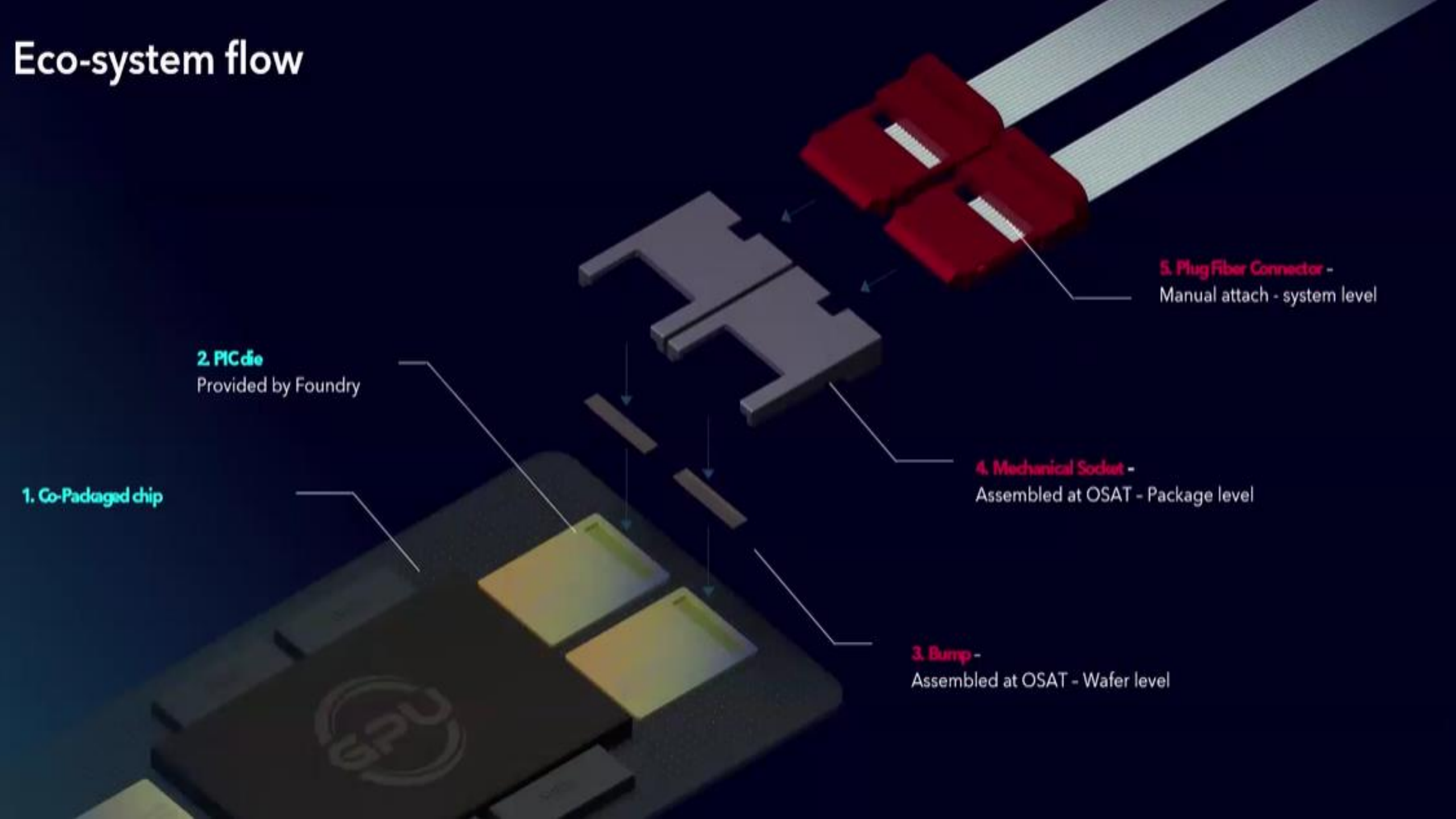
Detachable I/O coupler with Photonic-Plug & Photonic-Bump



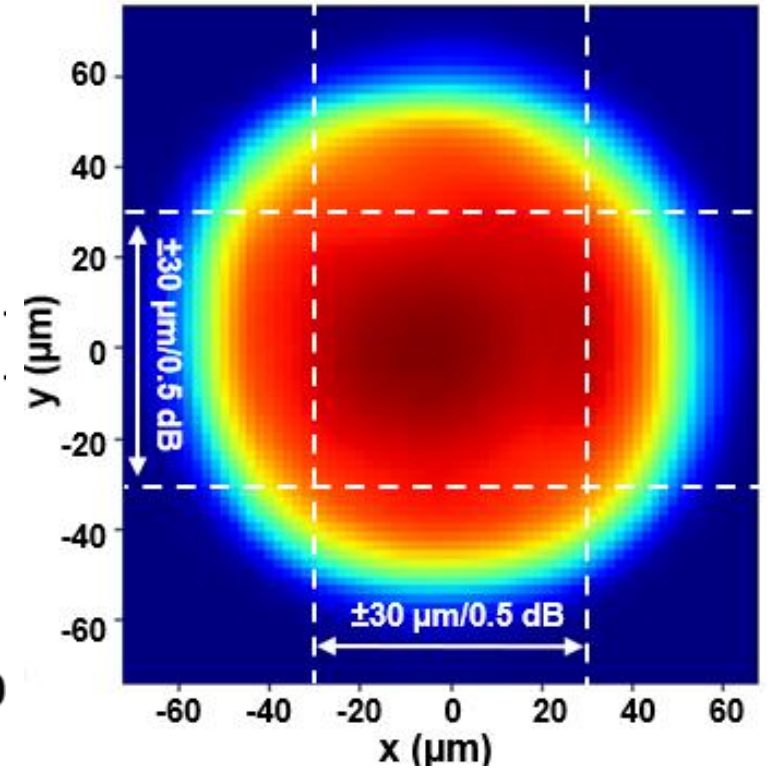
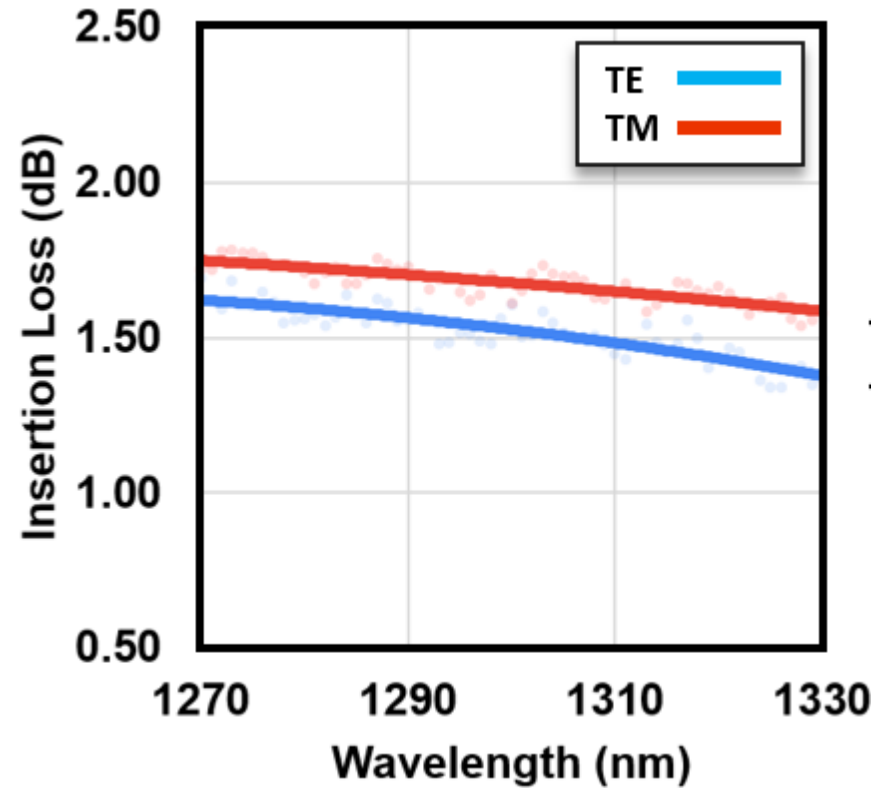
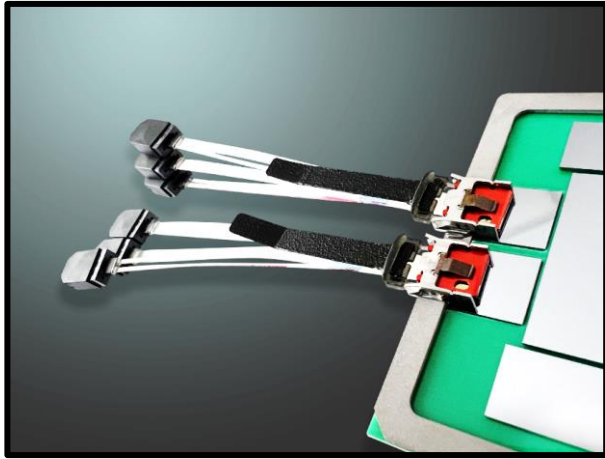
100x tolerance



Eco-system flow

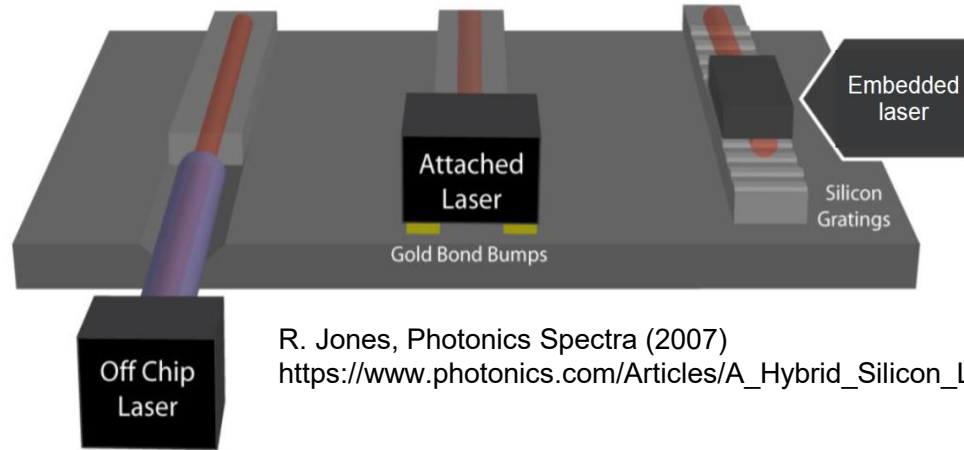


Detachable I/O coupler performance on GF platform



- Wafer-level detachable I/O solution (“reworkable”)
 - **Sub 1.8 dB IL** and broadband performance (flat through-band)
 - Lowest IL down to 1.3 dB
 - **+/- 30 μm 0.5 dB** misalignment tolerance
 - **+/- 45 μm 1 dB** misalignment tolerance

Laser Integration on SiPh Platform

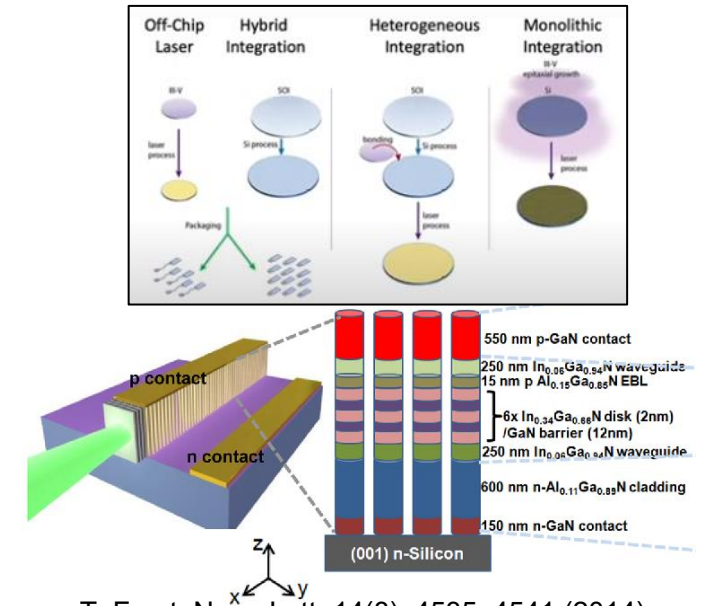


R. Jones, Photonics Spectra (2007)
https://www.photonics.com/Articles/A_Hybrid_Silicon_Laser/a27801

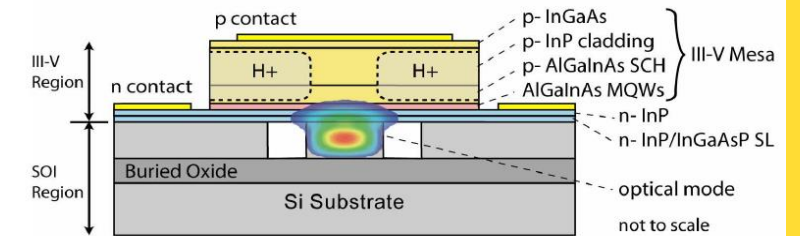
- ❑ Silicon is an indirect bandgap semiconductor
 - ✓ Highly inefficient light emission in the bulk material
- ❑ On-chip laser vs Off-chip laser
 - ✓ On-chip laser has the potential to reduce packaging costs by 60%
- ❑ III-V material integration for on-chip laser
 - ✓ Monolithic: Hetero-epitaxy
 - ✓ Heterogeneous: Direct wafer bonding
 - ✓ Hybrid: Flip-chip integration

**Challenge 1: Large divergence of III-V laser =>
Precise alignment in all dimensions**

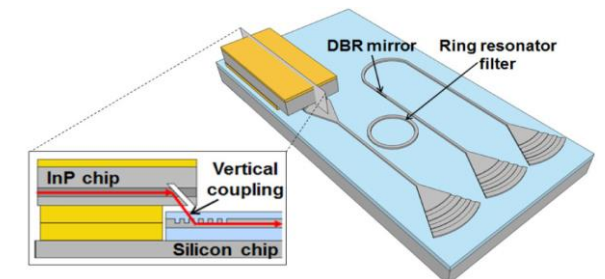
**Challenge 2: Significant mode mismatch =>
Elaborately designed intermediate coupling elements**



T. Frost, Nano Lett. 14(8), 4535–4541 (2014).

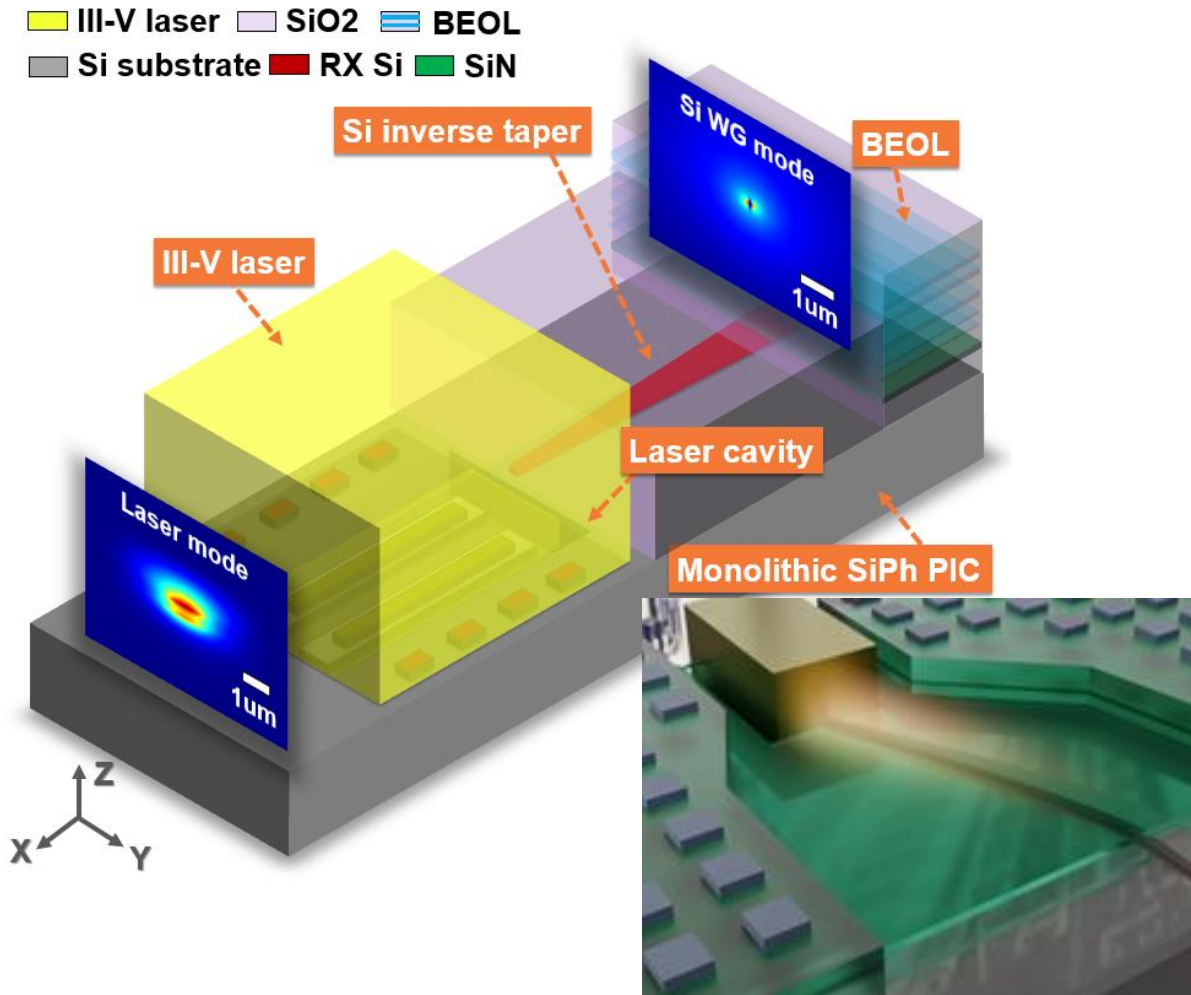


A. W. Fang, et al., Opt. Express 14(20), 9203–9210 (2006).



B. Song et al., Opt. Express 24 (10), 10435–10444 (2016).

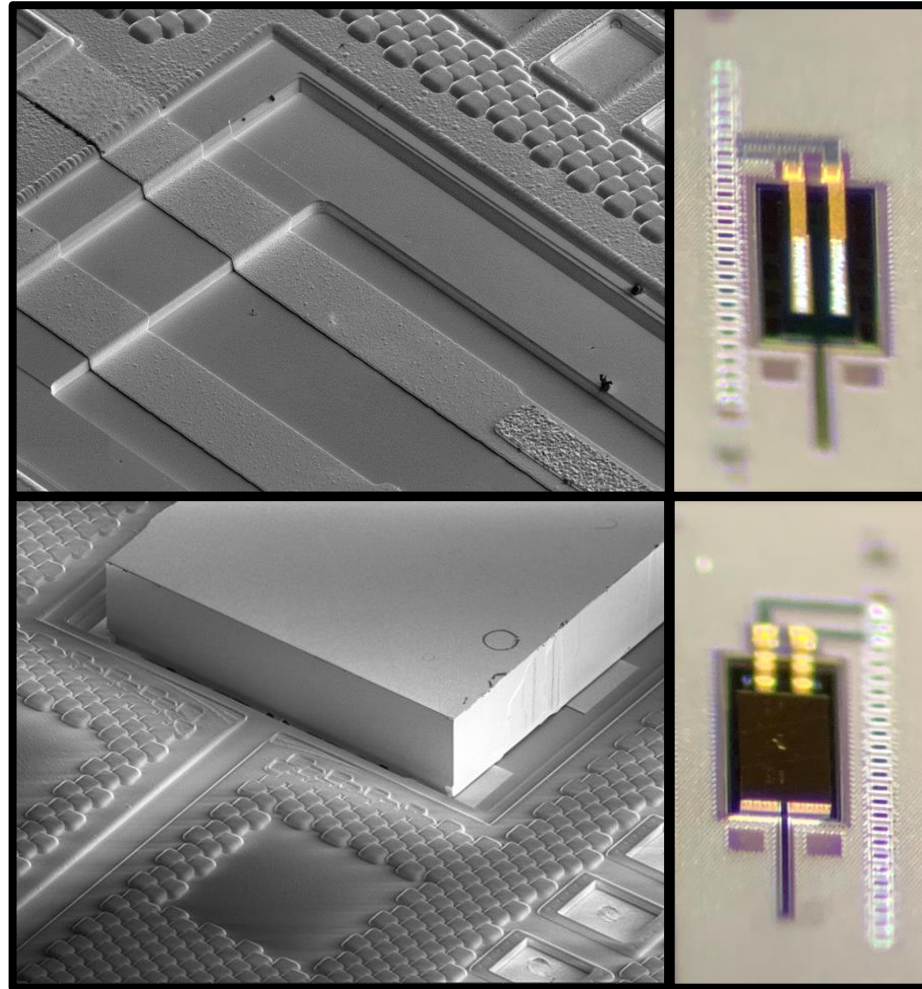
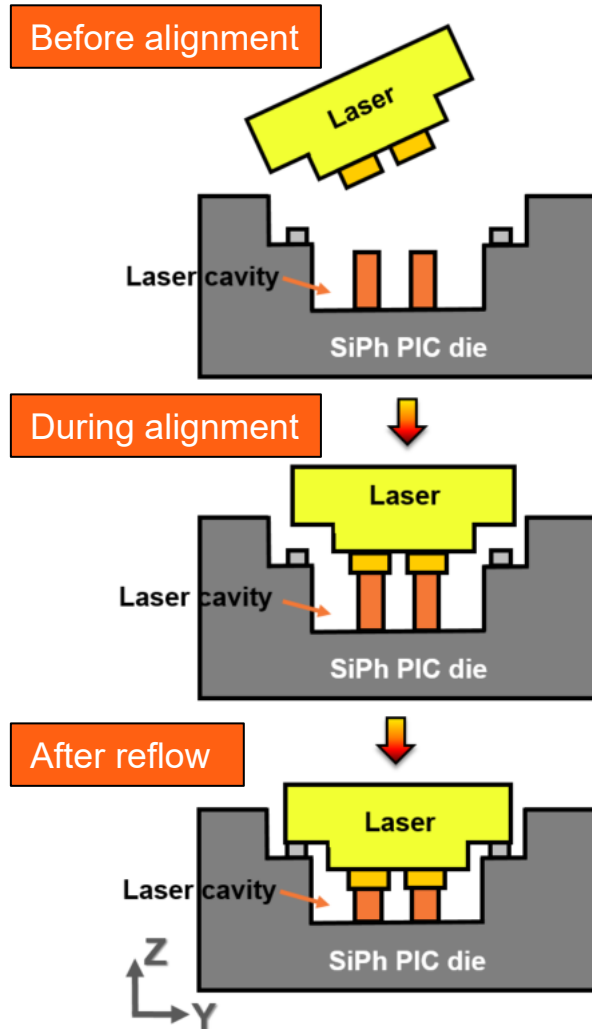
Hybrid Laser Integration on GF Monolithic SiPh Platform



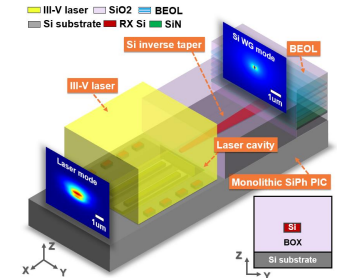
- ❑ Hybrid integration of laser on GF monolithic SiPh platform
- ✓ Flip-chip bonding of the laser diode inside the SiPh cavity
- ✓ Laser cavity formed during far back end of line (FBEOL) processing, co-optimized with laser provider
- ✓ Internal laser mode converter, co-optimized with SOI inverse taper
- ✓ Laser integrated with best-in-class active and passive SiPh devices including highly-efficient V-groove-integrated fiber attach

❑ Source: Y. Bian, OFC M5A.2 2021, Y. Bian, JSTQE 2023

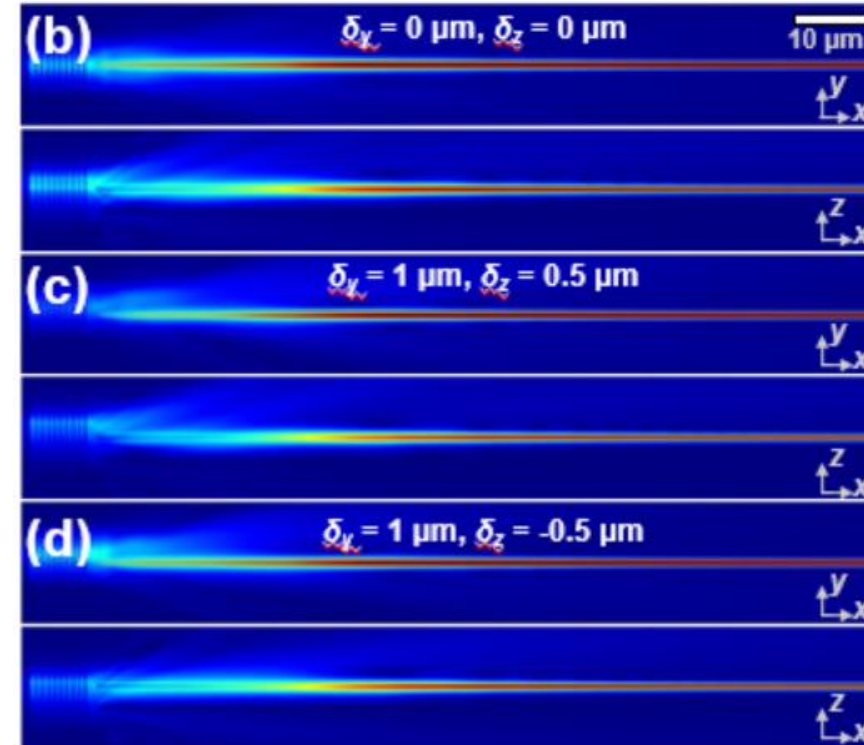
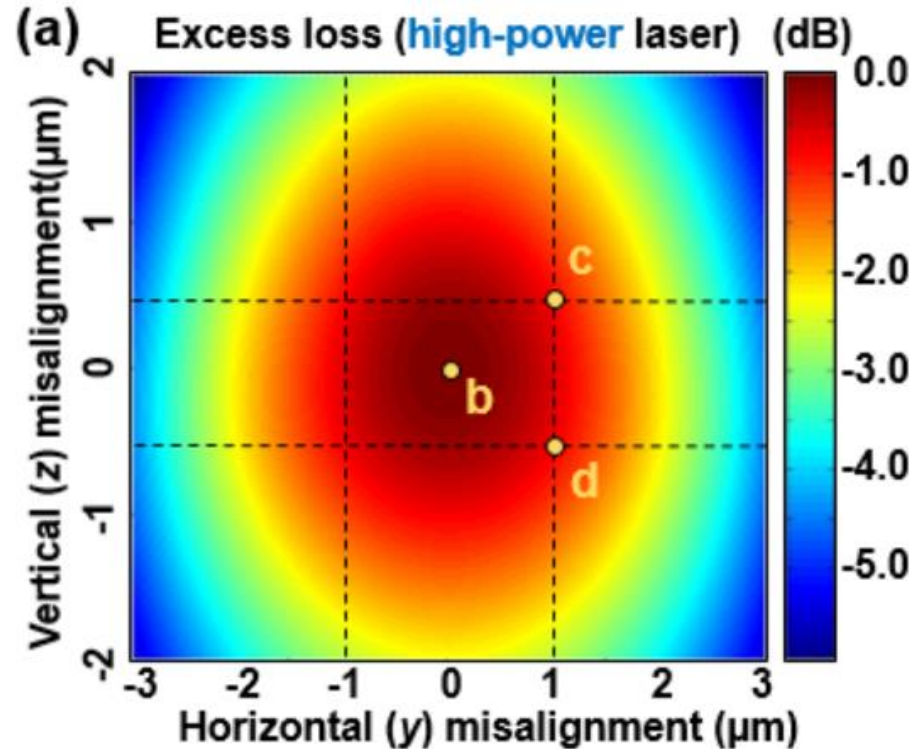
Flip-chip Laser Attach Process



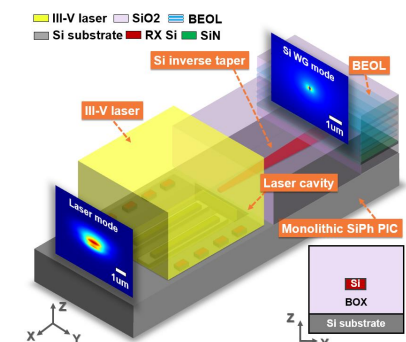
- ❑ High accuracy flip-chip laser attach through precise mechanical stops and optical alignment features
- ✓ Post fab processing to form wiring layers within the cavity and provide solder connections
- ✓ Passive z-alignment and seating of laser using high-precision mechanical stops inside the cavity of the PIC
- ✓ High precision bonding process for sub-micron alignment in x and y directions via optical alignment features



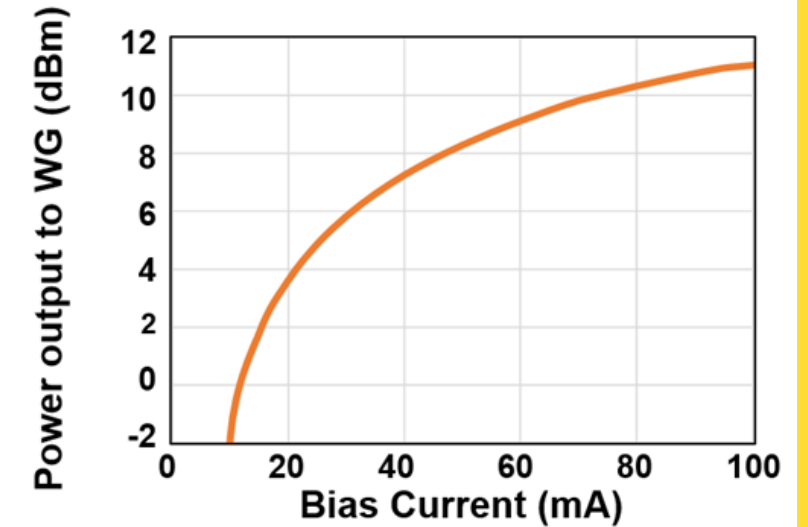
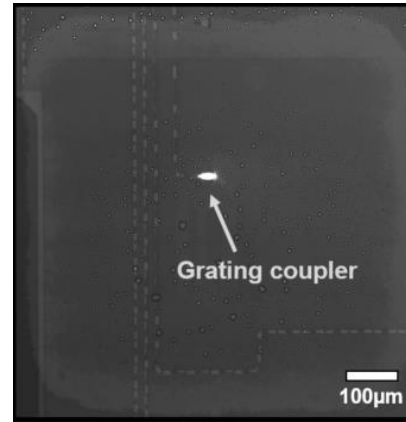
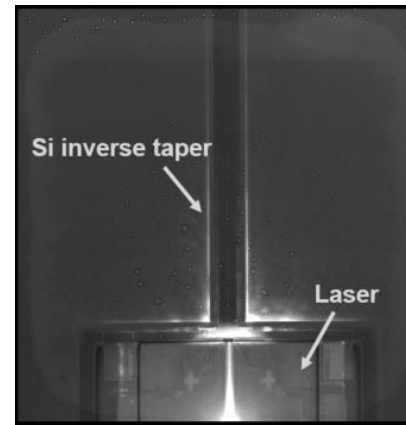
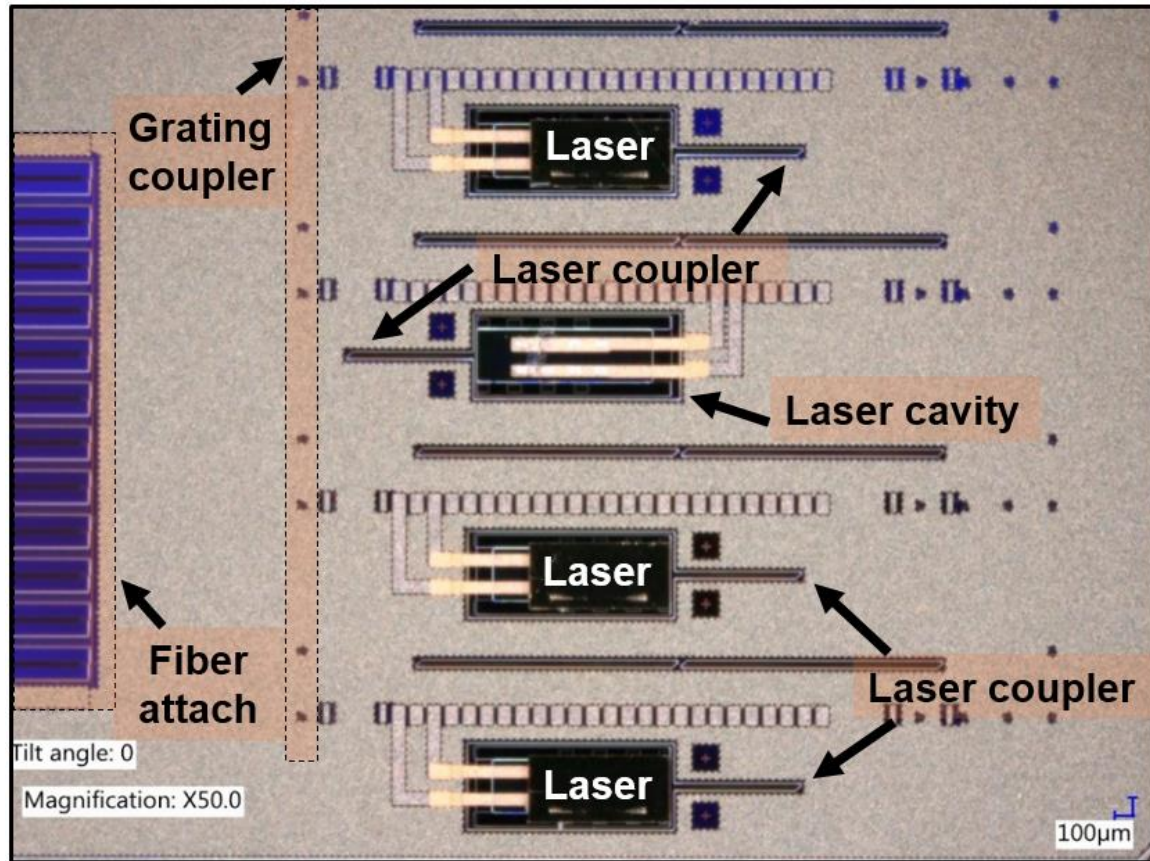
Laser Coupling Alignment Sensitivity – High-power Lasers



- ❑ Si SSC also performs well for **high-power** laser mode profile
- ❑ It provides a reasonable offset tolerance within the alignment capabilities of the attach tool used
 - ✓ Unique asymmetric alignment sensitivity contour due to different laser mode profiles
 - ✓ Less than 0.8 dB excess loss if the horizontal (y) and vertical (z) misalignment can be controlled within $\pm 1.0 \mu\text{m}$ and $\pm 0.5 \mu\text{m}$ (better than **low-power** lasers)



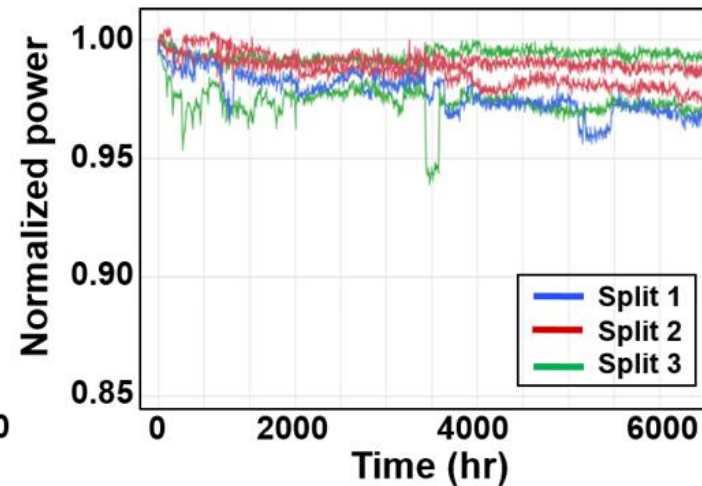
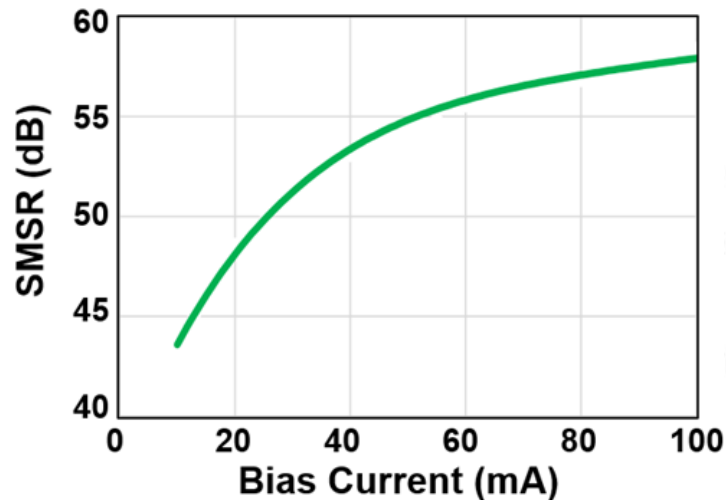
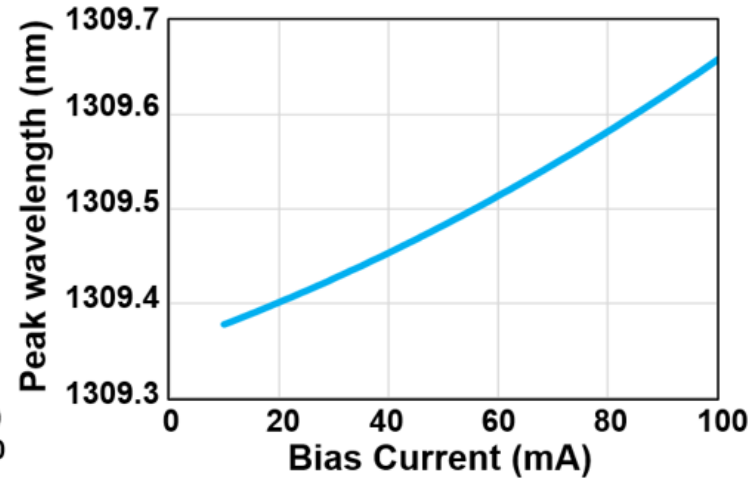
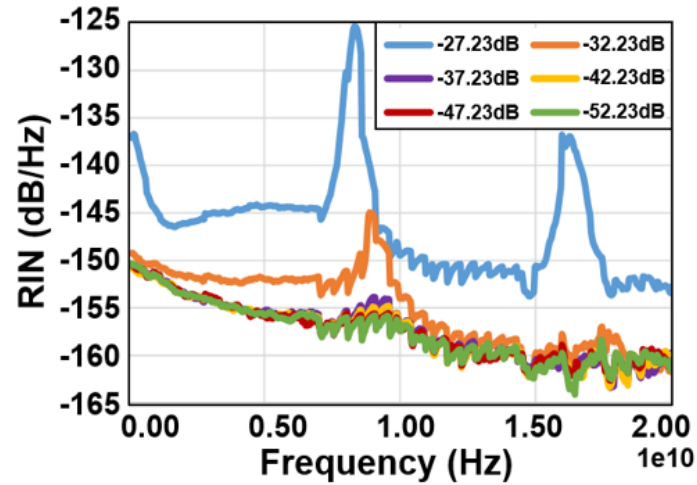
Laser Attach Chip & Wafer Level Tests



- ❑ Test chips built on monolithic SiPh platform
- ✓ Wafer level test: Optical paths from laser to grating coupler
- ✓ Chip level test: Optical paths from laser to V-groove fiber attach

- ❑ Wafer-level test
- ✓ Laser power output assessment
- ✓ Inverse taper conversion loss evaluation
- ❑ Chip-level test @ 1310 nm
- ✓ Input current limited to 100 mA
- ✓ > 12 dBm laser output power coupled to SiPh W

Laser Attach Experimental Results

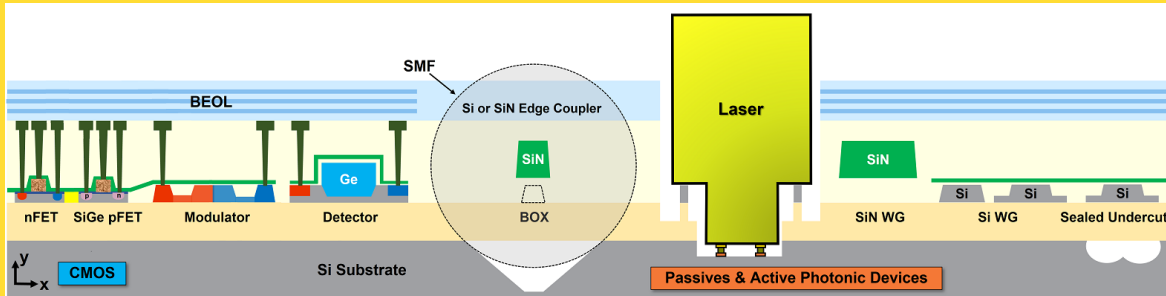


- ❑ **Module-level tests (RIN and mode hopping)**
 - ✓ RIN results => validated laser attach processes & other components in the PIC has no negative impact on RIN
 - ✓ Peak wavelength plot => module is mode-hop-free with no evidence of any wavelength discontinuity
 - ✓ The SMSR remains above 50 dB in the laser operating range => no mode competition
 - ✓ Development efforts continue to further mitigate mode hopping and improve yield performance
- ❑ **Early reliability assessments**
 - ✓ HTOL (Si submounts):
 - Bias current of 325 mA
 - Junction temperature of 110°C
 - Stable >5000 hours
 - ✓ Wafer-level ERA (laser attached SiPh cavity)
 - Temperature-humidity (TH) stress at 85°C
 - 85% relative humidity (RH) for > 1000 hours
 - Deep thermal cycling (-40°C to 85°C) > 500 hours
 - Stable performance throughout the stress-testing

❑ Ongoing activities

- Laser attach integrated with HP SiN coupler

Outline



- ❑ GF & 45SPCLO Technology Overview
- ❑ Photonics Device Library and Enhancements
- ❑ Edge couplers and Advanced Packaging
- ❑ **Fotonix™ PDK Enhancements**
- ❑ System-level Analyses and Circuit Demonstrations
- ❑ Summary and Outlook

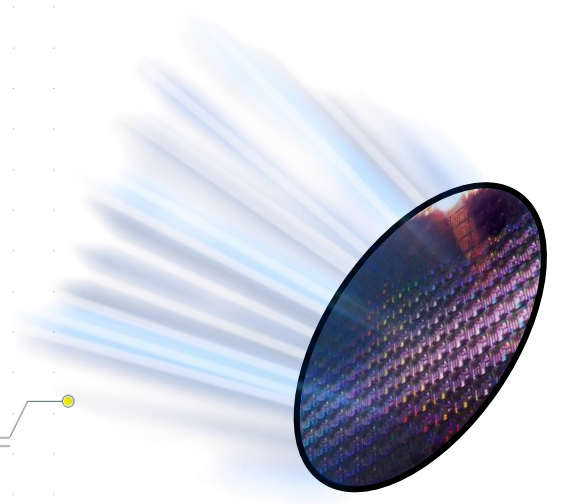
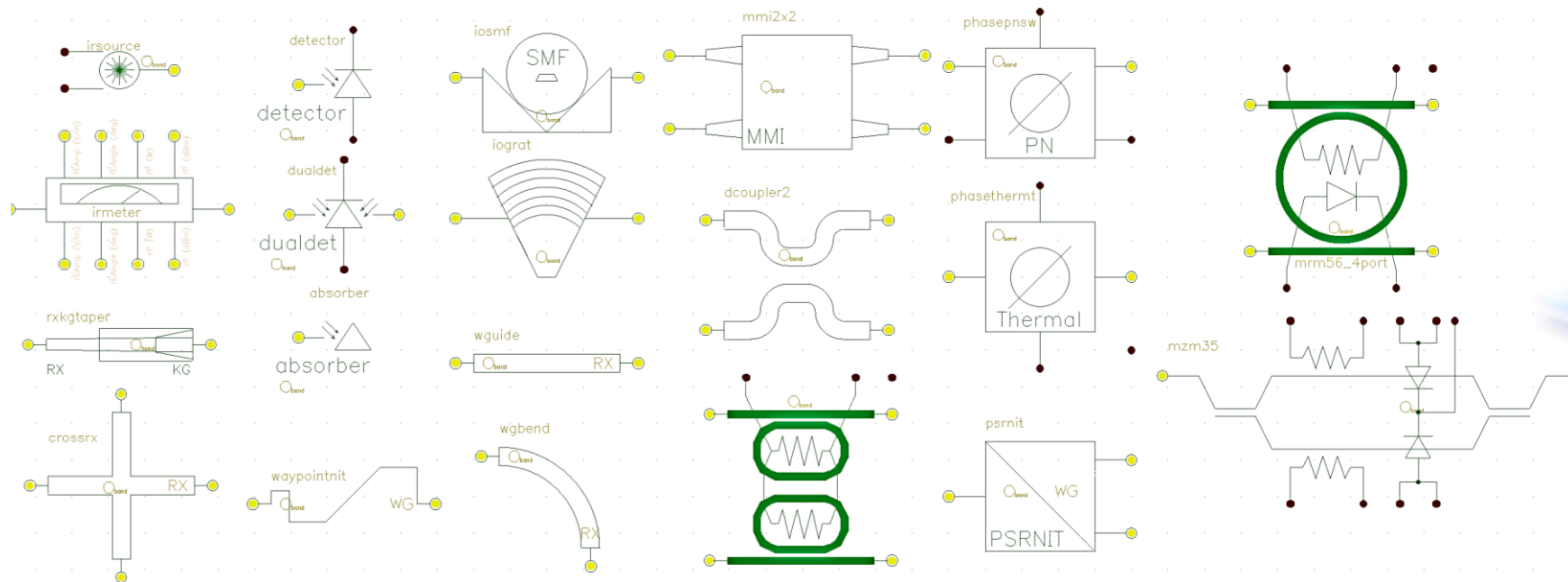
Comprehensive Photonic PDK Device Library

Compact Model Features

- **Hardware verified** and physics-based models
- Parameter, process variations (corner and Monte-Carlo simulations)
- Wavelength, temperature and optical power dependency
- Crosstalk and optical return loss (ORL)
- Supports bi-directionality

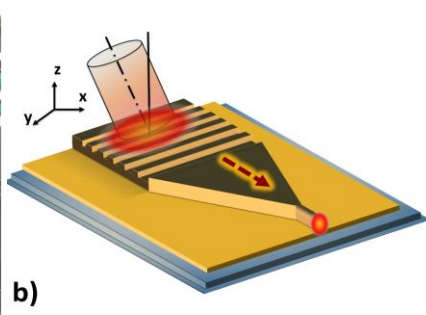
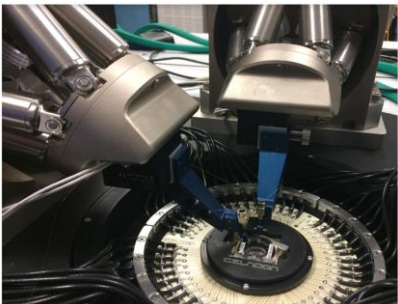
Highlights

- EO thermal time constant is modeled in all thermal phase shifters
- Thermal Coupling
- Photo-detector bandwidth and optical power influence
- Optical power self-heating in MRM
- Multi-channel models to support WDM simulations

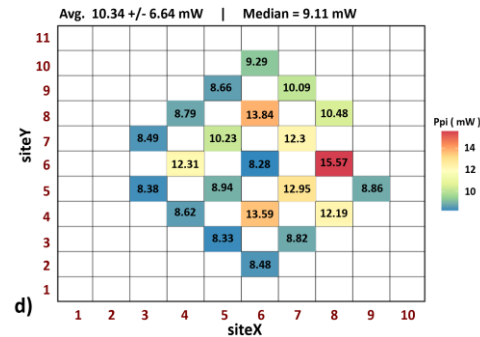
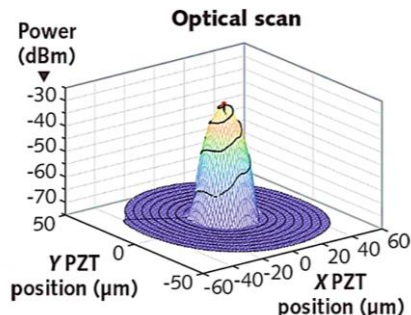


Source: Abdelsalam, OFC 2022; Qidi Liu, OFC 2024

Automated testing and characterization



b)



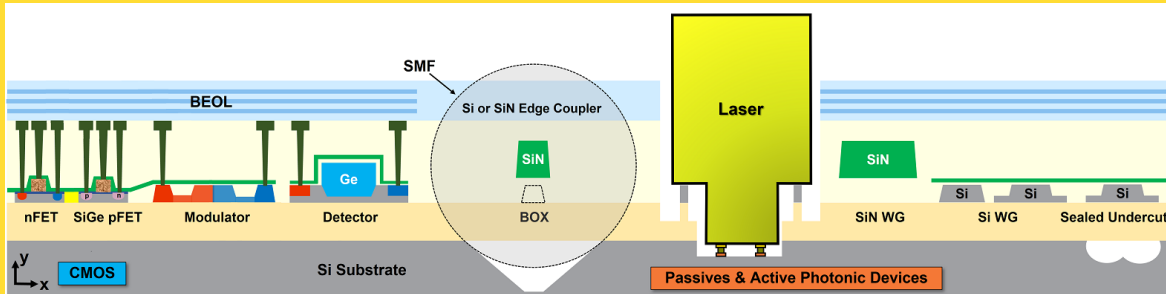
d)

Table 1. Key characterization parameters and measurement dependencies

		Dependency			
		Wavelength/Frequency	Voltage (V)	Temperature (C°)	Opt. power (dBm)
Measurements	Optical loss, insertion loss	O-band + C-band	0 : 20	-5 : 85	0 : 13
	V _π L , P _π	O-band + C-band	0 : 20	-5 : 85	0 : 13
	Pho-Current & Responsivity	O-band	0 : 20	-5 : 85	0 : 13
	Pho-Current & Responsivity	O-band	0 : 20	-5 : 85	0 : 13
	OE/EO BW	1310nm, 1550nm	0 : 20	25	0 : 13
	Eye-diag, Trans. response	1310nm,1550nm	(1.8V _{pp})	25	Optical amplifier
	DC I-V , C-V	-	max 200V, max 1A	(-40 : 150)	-
	AC EE S- <u>parm</u>	0.01GHz:110GHz	max 40V	(-40 : 150)	-

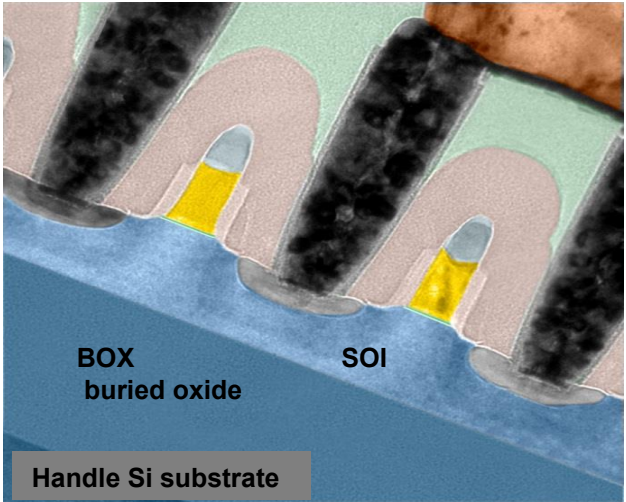
- Fully automated single and multi-modes optical fiber alignment with high precision moving stages
- Passive and active photonics devices can be tested using automated DC or RF probes with wavelength, temperature, voltage, optical power and frequency dependencies and light polarizations

Outline



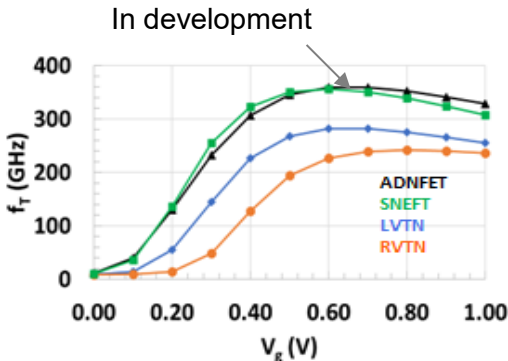
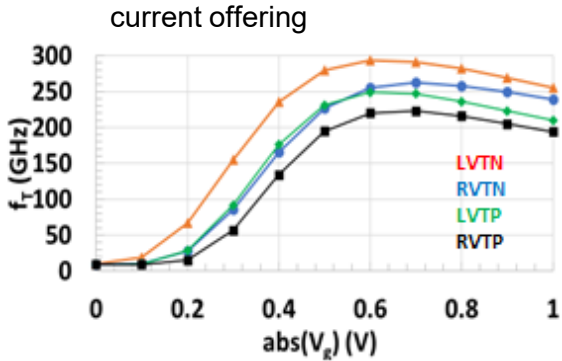
- ☐ GF & 45SPCLO Technology Overview
- ☐ Photonics Device Library and Enhancements
- ☐ Edge couplers and Advanced Packaging
- ☐ Fotonix™ PDK Enhancements
- ☒ **System-level Analyses and Circuit Demonstrations**
- ☐ Summary and Outlook

GF Fotonix™ High Performance Monolithic 45nm RF SOI CMOS



45nm partially depleted SOI CMOS integrated with photonics

300 GHz class analog mixed signal devices optimized for mmWave performance



Comprehensive digital standard cell library
High density / Low leakage

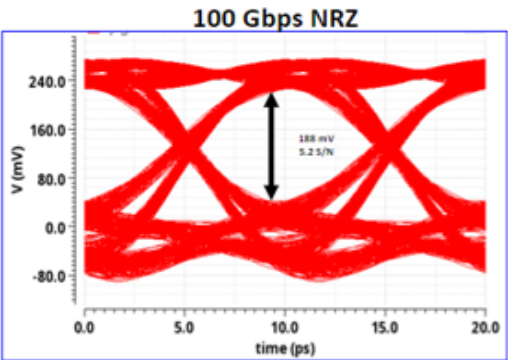
IP type	IP Detail
Standard Cell (9T) – RVT/UVT	477 RVT cells (24 High Perf cells), 449 UVT cells
1.8 GPIO (Flip Chip)	8 cells (Digital, Analog, ESD, Filler)
256 bit eFuse (32X8 bit)	Vdd: 0.9 – 1.16 V Temp range: -40 – 125C
Temperature Voltage Sensor	Temp range: -40 – 125C Voltage range: 0.8 - 1.1 V (Digital) 1.65 - 1.95V (Analog)

Enables high performance TIA's and Drivers monolithically integrated (EPIC)

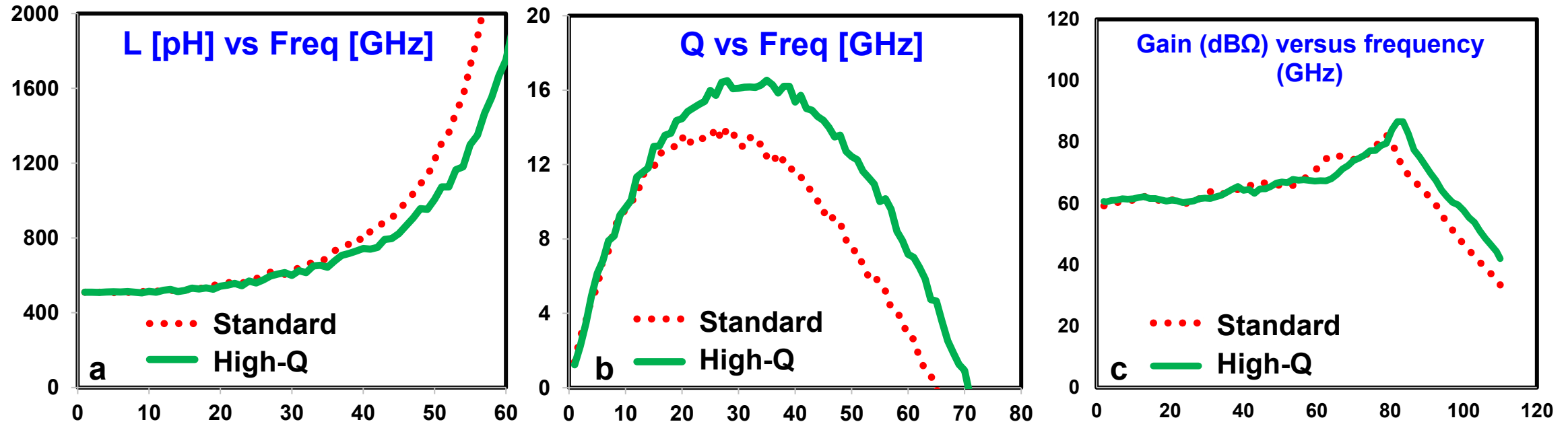
45SPCLO TIA – Simulation Results

	JSSC22*	MPW4C06 Simulation*
Technology	22nm FinFet	45SPCLO
Integration	hybrid	monolithic
Gain (dBQ)	59.3	61.8
Bandwidth (GHz)	45.5	88.5
CT (fF)	70	20
Noise density (pA/sqrt(Hz))	12.6	15.6
Power (mW)	11.2	14.3
FoM (Q.GHz/mW)	3781.7	7613.9

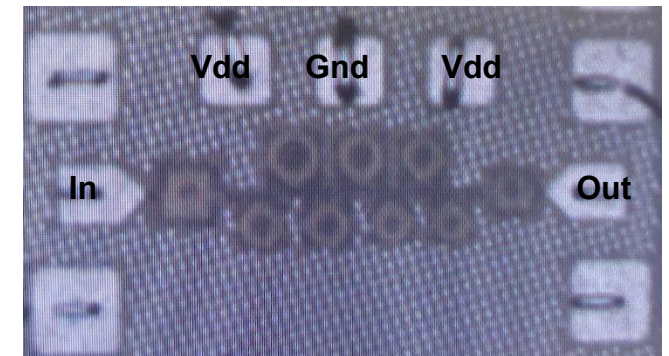
* Photodetector + EM on inductors + PEX LVT FET model
S. Daneshgar, H. Li, T. Kim and G. Balamurugan, "A 128 Gb/s, 11.2 mW Single-Ended PAM4 Linear TIA With 2.7 μ Arms Input Noise in 22 nm FinFET CMOS," in IEEE Journal of Solid-State Circuits, vol. 57, no. 5, pp. 1397-1408, May 2022, doi: 10.1109/JSSC.2022.3147467.



TIA bandwidth with optimized high-Q inductor measured to be 100 GHz

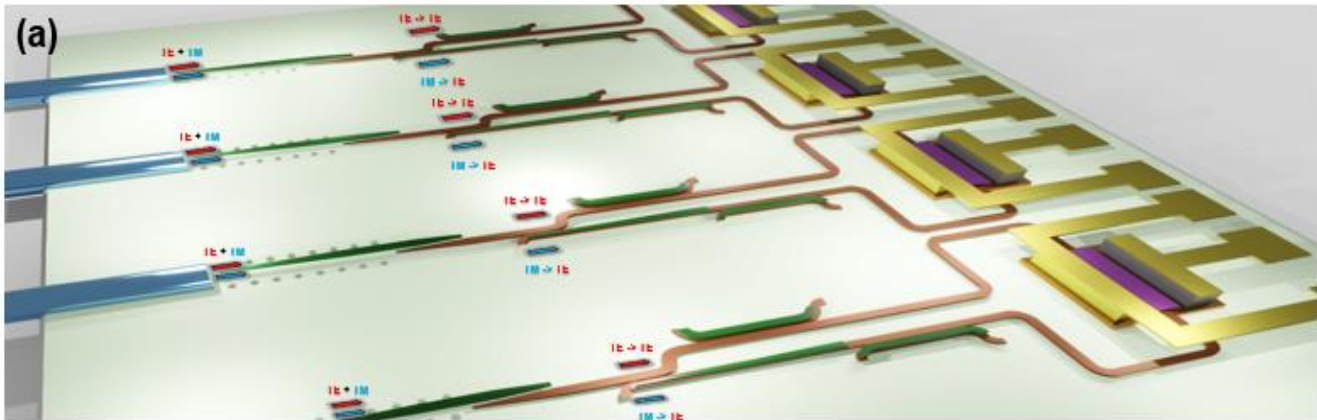


- Designed and measured on an MPW wafer with standard processing
- Q and self-resonant frequency of inductor increased by 18% and 9 %, respectively
- TIA bandwidth increased from 94 GHz to 100 GHz by using optimized high-Q inductor

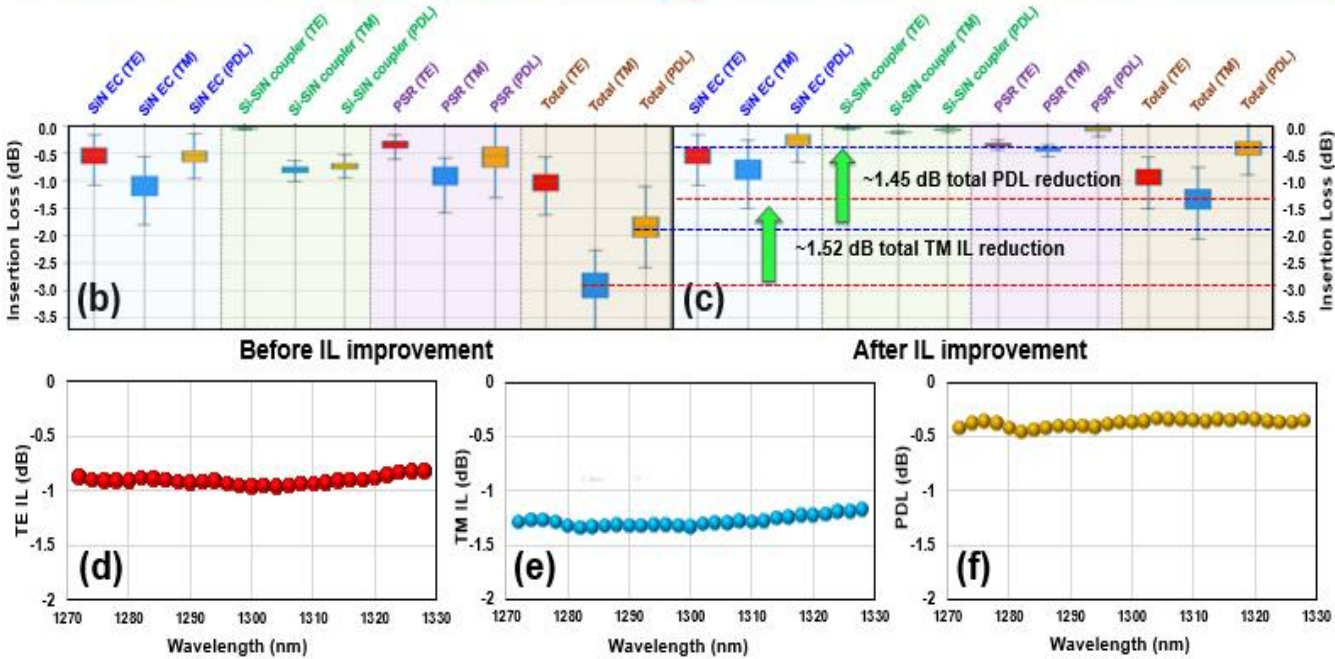


Chip micrograph of TIA design

IL & PDL reduction for monolithic optical receiver

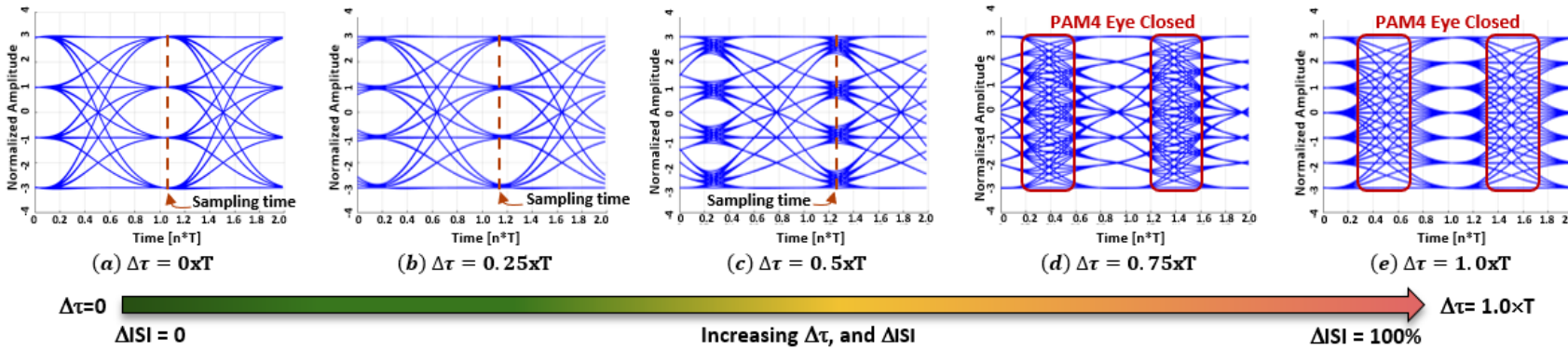


Component	TE IL (dB or dB/cm)	TM IL (dB or dB/cm)	PDL (dB or dB/cm)
SiN EC	0.6	0.8	0.2
Si-SiN coupler	0.049	0.11	0.061
PSR	0.34	0.42	0.08
Si WG	1.0	0.9	-0.1

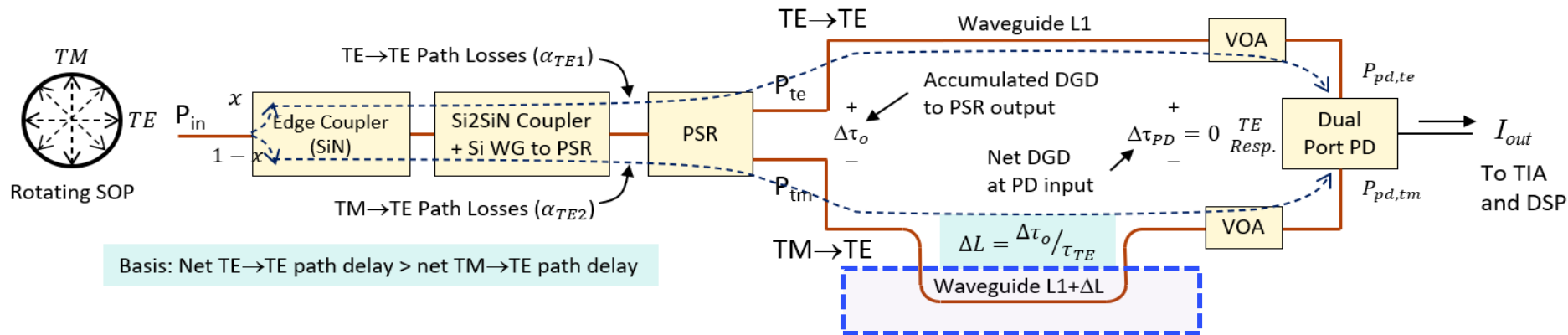


- Record high IL & PDL reduction
 - 1.52 dB reduction in overall TM IL
 - 1.45 dB reduction in PDL
 - Net PDL of merely **0.38 dB**
 - Broadband IL & PDL reduction
- Maintain integrity of monolithic SiPh platform
 - Performance improvements achieved through design and process optimizations without impacting the stack-up or introducing sophisticated circuits

DGD of SiPh component and system level impact



Component	DGD
SiN EC	0.05 ps
Si-SiN coupler	0.37 ps
PSR	5.2 ps
Si WG	5.3 ps/mm

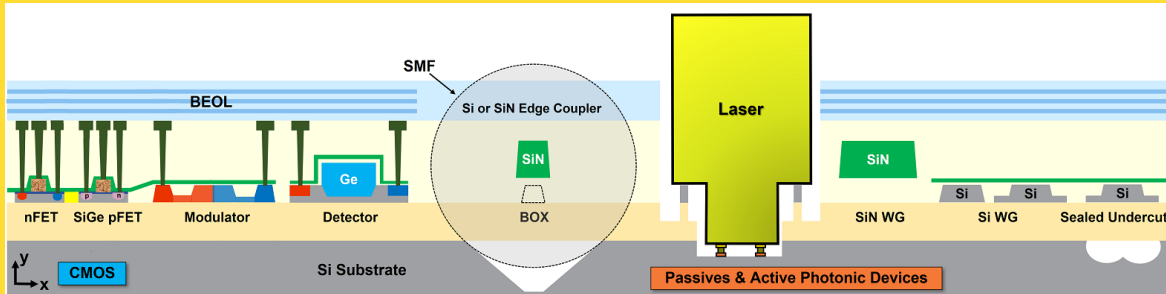


Left schematic shows TE→TE and TM→TE group delays from receiver input to dual port photodetector (PD)

- Substantial ISI introduced when DGD occupies a significant portion of PAM-4 symbol interval, leading to eye closure
- DGD compensation: the added waveguide length ΔL in faster TM→TE path equalizes the differential delay in the receive path to the dual port PD
- Note: any residual differential group delay from the fiber is to compensated by the equalizer in the DSP; VOA can be incorporated to fine tune the PDL

DGD: differential group delay
ISI: inter-symbol interference

Outline



- ❑ GF & 45SPCLO Technology Overview
- ❑ Photonics Device Library and Enhancements
- ❑ Edge couplers and Advanced Packaging
- ❑ Fotonix™ PDK Enhancements
- ❑ System-level Analyses and Circuit Demonstrations
- ❑ **Summary and Outlook**

PDK Access & Multi Project Wafers (MPW)

- 45SPCLO Process Design Kit (PDK) access is provided after NDA signature
- PDK access is provided through the customer account on the SFDC portal
- Technical or clarification questions relating to the technology or PDK can be submitted as a ticket through the GF Case system
 - The Technical Program Manager (TPM) will provide details on Case submission once the PDK access is approved
- MPW's are offered ~ 3X per year. One year look-ahead below.
- State-of-art wafer level optical & electrical test (WAC) is standard. Addition test services on request

Action	MPW#	MPW Region	Geometry	Reservation Close Date* ▼	Configurator Submit Date	Reservation Cancellation Deadline*
Raise MPW Request	MPW4C12	Non-Restricted	45SPCLO_45nm	8/20/2024	8/27/2024	9/17/2024
Raise MPW Request	MPW4C11	Non-Restricted	45SPCLO_45nm	4/16/2024	4/23/2024	5/14/2024
Raise MPW Request	MPW4C10	Non-Restricted	45SPCLO_45nm	12/19/2023	12/26/2023	1/16/2024

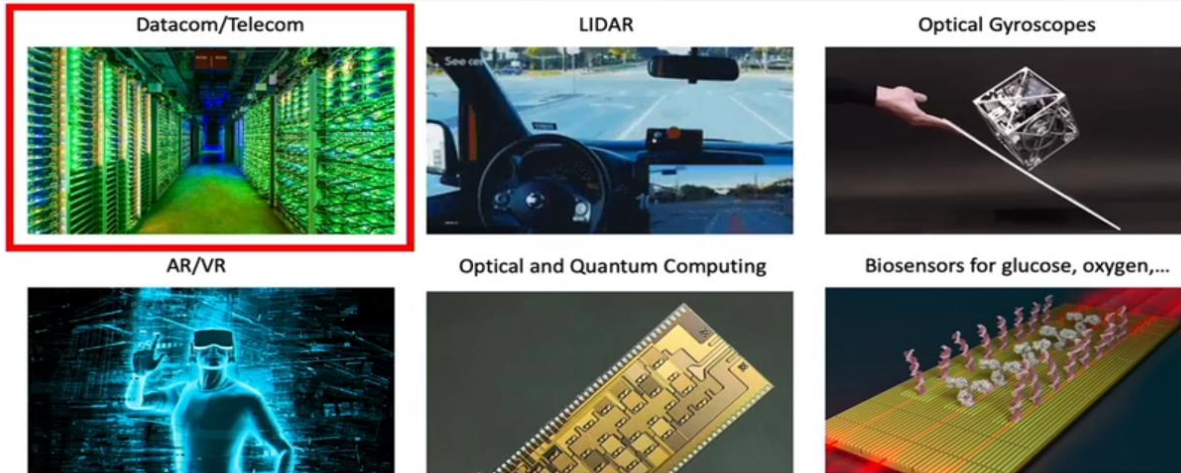
SiPh Foundry Challenges

- **Offering a PDK library that solutions a broad mix of PIC circuit architectures**
 - i.e. Various I/Os; different modulators (MRM, MZM), WDMs (cWDM, dWDM)
- **Rapid market & product requirements change**
 - High optical power input > 150mW (optical performance, reliability, etc.)
 - Higher electrical and optical BW to support applications beyond 200G
- **Broad mix of final package solution, lack of standardization**
 - Wire bond to Cu Pillar, Cu Pillar capture
 - Flip chip or PIC face up
 - Fiber attach methods for test and products
 - Rapid transition to Co-Packaged Optics
- **Mix of customers who want standard PDK pcells vs need for customization**
 - O-band & C-band custom device support including manufacturing and OPC
 - Custom packaging features

GF Fotonix™ roadmap & future directions

- Push to higher bandwidth supporting 200Gbit/s/lambda (PD, modulator & RF-CMOS)
- Finer pitch fiber attach 250 um -> 127um -> 65um
- Finer pitch Cu pillar supporting UCIe
- Connectorized fiber attach (pluggable/detachable I/O))
- 3D integration enablement
- Hybrid EIC co-design environment support
- Novel material integration, i.e. high-speed modulators, gain materials,...
- Continue support for customer's custom device designs
- Foundry solutions for marketplace beyond data centers

High Volume Billion Dollar Silicon Photonic Applications



Source: J. Bowers, OFC2022 Plenary Session

Silicon Photonics Innovation for Future Demands

Primary Market Driver:

- Data Center Interconnects
- HPC, Photonic Compute, AI
- Transition to Co-packaged optics

Secondary Markets:

- Quantum Compute
- Telecon
- Sensors, Lidar

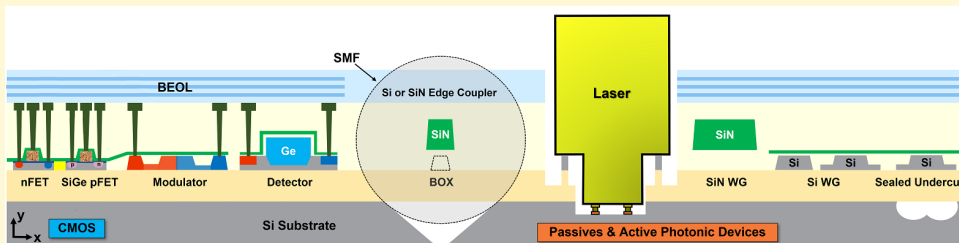
Future Opportunities...

- Defense harsh environment

Summary and Outlook

Latest Progress

- Comprehensive **passive and active** photonics libraries in addition to CMOS components
- Enhanced **SiN device suite** including CWDM measurement results
- High performance **SiN edge/surface coupler** including promising results on **32-channel** 127 μ m fiber attach with record low IL (0.4 dB) and pluggable coupler
- **Enhanced PDK compact models** and automated testing capabilities
- Demonstrated ORL reduction technique for high-speed PD with record high BW-Responsivity product **130 GHz*A/W**
- Measured **TIA BW** results up to **100 GHz**
- Demonstrated polarization insensitive receiver circuits with **minimal PDL and DGD**



Challenges and Future Directions

- **Challenges**
 - Offering a PDK library that solutions a broad mix of PIC circuit architectures
 - Rapid market & product requirements change
 - Broad mix of final package solution, lack of standardization
 - Mix of customers who want standard PDK pcells vs need for customization
- **Future directions**
 - **Higher bandwidth active** devices for 400 G/ λ
 - **Finer pitch** electrical and optical IO
 - **Connectorized** optical IO
 - **3D integration** enablement
 - Continued support for custom designs

Acknowledgements

- ❑ We would like to thank the entire **GlobalFoundries** team for their development engineering support for Fotonix™ technologies.



Takako Hirokawa, Won Suk Lee, Sujith Chandran, Michal Rakowski, Abdelsalam Aboketaf, Qidi Liu, Ming Gong, Bob Mulfinger, Ryan Sporer, Rick Carter, Ken Giewont, Ted Letavic, Kevin Dezuflian, Massimo Sorbara, Ryan Sporer, Bob Mulfinger, Michelle Zhang, Jae-Kyu Cho, Yarong Lin, Shenghua Song, Helen Wong, Zahidur Chowdhury, Arpan Dasgupta, Farid Barakat, Jason Kim, Kate McLean, Hanyi Ding, Jingyu Wu, Rongtao Cao, Fahimeh Banihashemian, Salman Mosleh, Chris Ritchie, Felix Beaudoin, Ryan Gallagher, Brian Popielarski, Francis O. Afzal, Mohamed Gheith, Ian Stobert, Mini Modh Ghosal, Prashanth Raghavendra Prasad, Ranjani Sirdeshmukh, Janet Tinkler, Frederick G. Anderson, Norm Robson, Seungman Choi, Andrea Paganini, Fen Jamin, Vaibhav Ruparelia, Ian Melville, George Gifford, Vikas Gupta, Kevin Soukup, Fab8 TD, Fab9 TD, Fab10 TD, Packaging Development Team, Design Enablement Team, Test Team, PDK Team, Reliability Team, Reference Design Team et al.

